(DSCO 11)

B.Sc. DEGREE EXAMINATION, MAY 2006
(Examination at the end of First Year)
Part II - Information Technology
Paper I : COMPUTER ORGANISATION

Time : Three hours Maximum : 100 marks

Answer any FIVE questions.
All questions carry equal marks.

1. (a) Design a sequential circuit wiht two JK Flip-Flops *P* and *Q* and two inputs x and y. If x = 0, the circuit remains in the same state regardless of the value of x. If x=y=1, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeat. When x=1 and y=0, the circuit goes through the state transition from 00 to 01 to 10 to 11 back to 00 and repeat.

   (b) Write down the characteristic tables and excitation tables for the following flip flops:
   (i) SR flip flop
   (ii) JK flip flop
   (iii) D flip flop
   (iv) T flip flop

2. (a) List in how many ways an integer can be represented.
   Prove the statement "An overflow is a problem in digital computers because the width of registers is finite".

   (b) Perform the subtraction with the following unsigned decimal numbers by taking 10's complement of the subtrahend.
   (i) 550 - 132
   (ii) 12 - 24
   (iii) 8753 - 1640.

3. (a) Provoke which of the following register transfer statements are wrong and why?
   (i) $xT : BR \leftarrow \overline{BR}, BR \leftarrow O$
   (ii) $yT : R4 \leftarrow R1, R4 \leftarrow R3, R4 \leftarrow R1 + R3$
   (iii) $zT : PC \leftarrow BR, PC \leftarrow PC + 1$

   (b) Illustrate shift micro-operations with a neat circuit diagram.

4. (a) Explain how interrupts are handled.

   (b) Evaluate the arithmetic statement

$$X = \frac{A + B - C * (D - E * F)}{G * H + K}$$

   using
   (i) Zero (ii) One (iii) Two (iv) Three address instructions.

5. (a) Illustrate the hardware implementation for signed magnitude addition and subtraction.

   (b) Get the product of (-12) and (7) using Booth's algorithm.

6. Explain the different modes of data transfer to and from peripherals in a digital computer.

7. (a) Explain the concept of "Locality of Reference" and its importance in the world of memory hierarchy.

(b) A two-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K x 31.

(i) Formulate all pertinent information required to construct cache memory.

(ii) What is the size of cache memory?

8. (a) Convert the following into polish and reverse polish notations:

(i) $A*B+A*(B*D+C*E)$

(ii) $\frac{A*[B+C*(D+E)]}{F*(G+H)}$

(iii) $(3+4)[10(2+6)+8]$.

(iv) $A+B*[C*D+E*(F+G)]$

(b) Distinguish between a Branch instruction, a call sub-routine instruction and program interrupt.

9. (a) Differentiate combinational and sequential circuits with suitable examples for each of them.

(b) Explain the algorithm for 2's complement division with flow chart and also with an example.

10. (a) Design an array multiplier that multiplies two 4-bit numbers using AND gates and Binary Address.

(b) Discuss how Input-Output processor act as an interface between CPU and external devices.

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