(EM 314)

III/IV B.Tech. DEGREE EXAMINATION, OCTOBER 2005.

First Semester

VHDL

Time : Three hours Maximum : 70 marks

Answer Question No.1 compulsorily. (7 × 2 = 14)

Answer ONE question from each Unit. (4 × 14 = 56)

All questions carry equal marks.

1. (a) What is a typical design flow for designing VLSI IC circuits?

(b) Difference between top – down and bottom – up design methodologies for digital design.

(c) What are the logic value set and data types such as any nets, registers and numbers?

(d) Explain the port connection rules in a module instantiation.

(e) What are fall and turn–off delays in the gate–level design?

(f) Enumerate the continuous assignments (assign) statement and restrictions on the assign statement.

(g) Give the significance of structured procedures always and initial in behavioral modeling.

UNIT I

2. (a) Explain the following basic VHDL building blocks :

(i) Entity

(ii) Architecture

(iii) Configuration

(iv) Driver.

Or

(b) Write the following variables in VHDL.

(i) An 8–bit vector net called a_in.

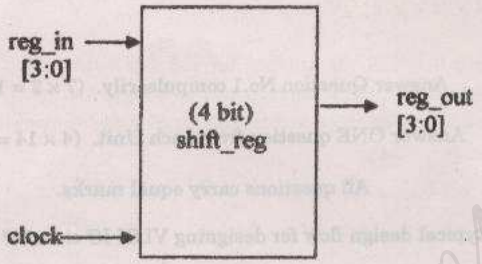
(ii) A 32–bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32–bit decimal number equal to 3.

(iii) A time variable called snap_shot.

(iv) A memory MEM containing 256 words of 64 bits each.

UNIT II

3. (a) Describe how signal assignments are the most basic form of VHDL with suitable examples A 4–bit parallel shift register has I/O pins as shown in the figure below. Write the module definition for this module shift_reg. Include the list of ports and port declarations. You do not need to show the internals.



Or

(b) Explain how subprograms consist of functions and procedures with examples.

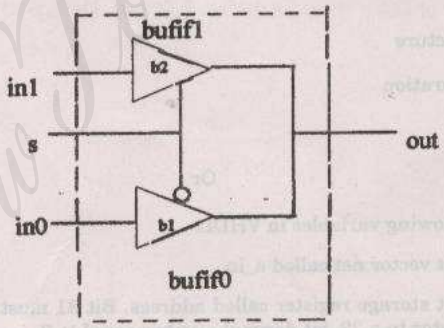
(c) Describe how functions can be used as resolution functions to calculate the proper value on a multiple driven or iterative network.

UNIT III

4. (a) With the help of suitable examples, explain how types can be used by three different types of objects: the signal, variable and constant. Explain how enumerated types can be used to describe user–defined operations and make a model much more readable.

Or

(b) Design a 2–to–1 multiplexer using bufif0 and bufif1 gates as shown below :



Assume suitable delay specification for gates b1 and b2. Apply stimulus and test the output values.

UNIT IV

5. (a) A full subtractor has three 1–bit inputs x,y and z (previous borrow) and two 1–bit outputs D(difference) and B(borrow). The logic equations for D and B are as follows :

$$D = x'.y'.z + x'.y.z' + x.y'.z' + x.y.z$$

$$B = x'.y + x'.z + y.z$$

Write the full VHDL description for the full subtractor module, including I/O ports (Remember that + in logic equations corresponds to a logical or operator in dataflow). Instantiate the subtractor inside a stimulus block and test all eight possible combinations of x, y and z given in the following truth table.

X	Y	Z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Or

(b) Design a negative edge–triggered D–flip–flop (D_FF) with synchronous clear, active high D_FF clears only at a negative edge of clock when clear is high). Use behavioral statements only. (Hint : Output q of D_FF must be declared as reg). Design a clock with a period of 10 units and test the D–FF.
