ANNA UNIVERSITY COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : MAY / JUNE 2010

REGULATIONS : 2007

SIXTH SEMESTER : ELECTRONICS & COMMUNICATION ENGINEERING

070290070 - VLSI DESIGN

TIME : 3 Hours **Max.Marks : 100**

PART – A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. Define Layout Editor
2. What is Reactive Ion Etching (RIE)?
3. Define Yield
4. Draw the PFET masking sequence
5. List the classifications of design rules
6. Give the equation for PFET resistance Rp
7. Write the level1 SPICE MOSFET parameters
8. Define Body bias
9. Draw the circuit diagram of Tristate Inverter
10. Write the sum and carryout equation of full-adder
11. Draw the layout of a 2-Input NOR gate by using CMOS logic
12. Define drift current
13. Define threshold and give the threshold equation for nFET structure
14. What is ring Oscillator?
15. Why charge leakage occurs in CMOS circuits?
16. What do you mean by domino logic?
17. Write the syntax for FOR/GENERATE Statement
18. Compare Signal and Variable
19. List the syntax of WAIT UNTIL statement with example
20. Define sensitivity list for Process statement.

PART - B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. a. Give the step-by step evolution of the chip from bare Silicon wafer to the finished product based on CMOS fabrication (8)

    b. Discuss in brief the operation of basic NMOS enhancement transistor (4)

22. a. Write the SCMOS design rules for N-well,P-diffusion,Poly1,Contacts, Metal 1 and Via1 layers (8)

    b. Define Photolithography. Give the sequence used to create the pattern (4)

23. a. Discuss in detail about the electrical & transient characteristics of CMOS Inverter (8)

    b. What do you mean by latch-up in CMOS circuits and give certain remedies for the latch-up problem (4)

24. a. Realize the following function using complex logic gates (8)

    i) $g = \overline{a.b+c.d}$ ii) $h = \overline{(a+b).(c+d)}$

    b. Draw the Euler graph for the function F=(a+b).c (4)

25. a. Explain the function of static RAM cell with its SPICE Simulation (8)

    b. With neat diagram explain the function of Master-Slave D-type flip-flop (4)

26. a. Write a VHDL code for a 4-to-1 multiplexer by using CASE Statement. (6)

b. Write a VHDL code for a 8x3 encoder by using WHEN/ELSE Statement (6)

27. a. Write a VHDL program for a Mealy state machine in any one modeling (8)

b. Compare Concurrent and Sequential Statement (4)

28. a. Explain in detail about the Transmission gates and pass logic (8)

b. Briefly explain about series connected FETs. (4)

*****THE END*****