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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEEING

TWO MARK QUESTIONS WITH ANSWERS (For ALL units)

SUBJECT NAME : DIGITAL SYSTEMS

SUBJECT CODE : CS1202

CLASS : S3 (B.E) CSE

1.Define the term digital.

The term digital refers to any process that is accomplished using discrete units

2.What is meant by bit?

A binary digit is called bit

3.What is the best example of digital system?

Digital computer is the best example of a digital system.

4.Define byte?

A group of 8 bits.

5.List the number systems?

i) Decimal Number system
ii) Binary Number system
iii) Octal Number system
iv) Hexadecimal Number system

6.State the sequence of operator precedence in Boolean expression?

i) Parenthesis
ii) AND
iii) OR

7.What is the abbreviation of ASCII and EBCDIC code?

ASCII-American Standard Code for Information Interchange.
EBCDIC-Extended Binary Coded Decimal Information Code.

8.What are the universal gates?

NAND and NOR

9.What are the different types of number complements?

i) r's Complement
ii) (r-1)'s Complement.

10.Why complementing a number representation is needed?

Complementing a number becomes as in digital computer for simplifying the subtraction operation and for logical manipulation complements are used.

11.How to represent a positive and negative sign in computers?

Positive (+) sign by 0
Negative (-) sign by 1.

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12.What is meant by Map method?

The map method provides a simple straightforward procedure for minimizing Boolean function.

13.What is meant by two variable map?

Two variable map have four minterms for two variables, hence the map consists of four squares, one for each minterm

14.What is meant by three variable map?

Three variable map have 8 minterms for three variables, hence the map consists of 8 squares, one for each minterm

15.Which gate is equal to AND-inverter Gate?

NAND gate.

16.Which gate is equal to OR-inverter Gate?

NOR gate.

17.Bubbled OR gate is equal to----------

NAND gate

18. Bubbled AND gate is equal to----------

NOR gate

19.What is the use of Don't care conditions?

Any digital circuit using this code operates under the assumption that these unused combinations will never occur as long as the system

.

20.Express the function f(x, y, z)=1 in the sum of minterms and a product of maxterms?

Minterms=∑(0,1,2,3,4,5,6,7)

Maxterms=Nomaxterms.

21.What is the algebraic function of Exclusive-OR gate and Exclusive-NOR gate?

$F=xy^1 + x^1y$

$F=xy + x^1y^1$

22.What are the methods adopted to reduce Boolean function?

i) Karnaugh map

ii) Tabular method or Quine mccluskey method

iii) Variable entered map technique.

23.Why we go in for tabulation method?

This method can be applied to problems with many variables and has the advantage of being suitable for machine computation.

24.State the limitations of karnaugh map.

i) Generally it is limited to six variable map (i.e.) more then six variable involving expressions are not reduced.

ii) The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

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25.What is tabulation method?

A method involving an exhaustive tabular search method for the minimum expression to solve a Boolean equation is called as a tabulation method.

26.What are prime-implicants?

The terms remained unchecked are called prime-implecants. They cannot be reduced further.

27.Explain or list out the advantages and disadvantages of K-map method?

The advantages of the K-map method are

i. **It is a fast method for simplifying expression up to four variables.**
ii. **It gives a visual method of logic simplification.**
iii. **Prime implicants and essential prime implicants are identified fast.**
iv. **Suitable for both SOP and POS forms of reduction.**
v. **It is more suitable for class room teachings on logic simplification.**

The disadvantages of the K-map method are

i. **It is not suitable for computer reduction.**
ii. **K-maps are not suitable when the number of variables involved exceed four.**
iii. **Care must be taken to fill in every cell with the relevant entry, such as a 0, 1 (or) don't care terms.**

28.List out the advantages and disadvantages of Quine-Mc Cluskey method?

The advantages are,

a. **This is suitable when the number of variables exceed four.**
b. **Digital computers can be used to obtain the solution fast.**
c. **Essential prime implicants, which are not evident in K-map, can be clearly seen in the final results.**

The disadvantages are,

a. **Lengthy procedure than K-map.**
b. **Requires several grouping and steps as compared to K-map.**
c. **It is much slower.**
d. **No visual identification of reduction process.**
e. **The Quine Mc Cluskey method is essentially a computer reduction method.**

29.Define Positive Logic.

When high voltage or more positive voltage level is associated with binary '1' and while the low or less positive level is associated with binary '0' then the system adhering to this is called positive logic.

30.Define Negative Logic.

When high voltage level is associated with binary '0' and while the low level is associated with binary '1' then the system adhering to this is called negative logic

31.List the characteristics of digital Ics

i) **propagation delay**
ii) **power dissipation**
iii) **Fan-in**

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iv) Fan-out
v) Noise margin

32.What is propagation delay?

It is the average transition delay time for the signal to propagate from input to output when the signals change in value.

33.What is Noise margin?

It is the limit of a noise voltage, which may be present with out impairing the proper operation of the circuit.

34.What is power dissipation?

It is the power consumed by the gate, which must be available from the power supply.

35.Why parity checker is needed?

Parity checker is required at the receiver side to check whether the expected parity is equal to the calculated parity or not. If they are not equal then it is found that the received data has error.

36.What is meant by parity bit?

Parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message, including the parity bit is transmitted and then checked at the receiving and for errors.

37.Why parity generator necessary?

Parity generator is essential to generate parity bit in the transmitter.

38.What is IC?

An integrated circuit is a small silicon semiconductor crystal called a chip containing electrical components such as transistors, diodes, resistors and capacitors. The various components are interconnected inside the chip to form an electronic circuit.

39.What are the needs for binary codes?

a. Code is used to represent letters, numbers and punctuation marks.
b. Coding is required for maximum efficiency in single transmission.
c. Binary codes are the major components in the synthesis (artificial generation) of speech and video signals.
d. By using error detecting codes, errors generated in signal transmission can be detected.
e. Codes are used for data compression by which large amounts of data are transmitted in very short duration of time.

40.Mention the different type of binary codes?

The various types of binary codes are,

f. BCD code (Binary Coded decimal).
g. Self-complementing code.
h. The excess-3 (X's-3) code.
i. Gray code.
j. Binary weighted code.
k. Alphanumeric code.
l. The ASCII code.
m. Extended binary-coded decimal interchange code (EBCDIC).

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n. Error-detecting and error-correcting code.
o. Hamming code.

41.List the advantages and disadvantages of BCD code?

The advantages of BCD code are

a. Any large decimal number can be easily converted into corresponding binary number
b. A person needs to remember only the binary equivalents of decimal number from 0 to 9.
c. Conversion from BCD into decimal is also very easy.

The disadvantages of BCD code are

a. The code is least efficient. It requires several symbols to represent even small numbers.
b. Binary addition and subtraction can lead to wrong answer.
c. Special codes are required for arithmetic operations.
d. This is not a self-complementing code.
e. Conversion into other coding schemes requires special methods.

42.What is meant by self-complementing code?

A self-complementing code is the one in which the members of the number system complement on themselves. This requires the following two conditions to be satisfied.

a. The complement of the number should be obtained from that number by replacing 1s with 0s and 0s with 1s.
b. The sum of the number and its complement should be equal to decimal 9. Example of a self-complementing code is
   i. 2-4-2-1 code.
   ii. Excess-3 code.

43.Mention the advantages of ASCII code?

The following are the advantages of ASCII code

a. There are 2^7 =128 possible combinations. Hence, a large number of symbols, alphabets etc.., can be easily represented.
b. There is a definite order in which the alphabets, etc.., are assigned to each code word.
c. The parity bits can be added for error-detection and correction.

44.What are the disadvantages of ASCII code?

The disadvantages of ASCII code are

a. The length of the code is larger and hence more bandwidth is required for transmission.
b. With more characters and symbols to represent, this is not completely sufficient.

45.What is the truth table?

A truth table lists all possible combinations of inputs and the corresponding outputs.

46.Define figure of merit?

Figure of merits is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nano seconds.

Figure of merits=Propagation delay time (ns)*

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Power (mw)

It is specified in pico joules (ns*mw=PJ).

47.What are the two types of logic circuits for digital systems?

Combinational and sequential

48.Define Combinational circuit.

A combinational circuit consist of logic gates whose outputs at anytime are determined directly from the present combination of inputs without regard to previous inputs.

49.Define sequential circuits.

Their outputs are a function of the inputs and the state of memory elements. The state of memory elements, in turn, is a function of previous inputs.

50.What is a half-adder?

The combinational circuit that performs the addition of two bits are called a half-adder.

51.What is a full-adder?

The combinational circuit that performs the addition of three bits are called a half-adder.

52.What is half-subtractor?

The combinational circuit that performs the subtraction of two bits are called a half-sub tractor.

53.What is a full-subtractor?

The combinational circuit that performs the subtraction of three bits are called a half- sub tractor.

54.What is Binary parallel adder?

A binary parallel adder is a digital function that produces the arithemetic sum of two binary numbers in parallel.

55.What is BCD adder?

A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit also in BCD.

56.What is Magnitude Comparator?

A Magnitude Comparator is a combinational circuit that compares two numbers, A and B and determines their relative magnitudes.

57.What is decoder?

A decoder is a combinational circuit that converts binary information from 'n' input lines to a maximum of 2^n unique output lines.

58.What is encoder?

A decoder is a combinational circuit that converts binary information from 2^nInput lines to a maximum of 'n' unique output lines.

59.Define Multiplexing?

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Multiplexing means transmitting a large number of information units over a smaller number of channels or lines.

60.What is Demultiplexer?

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines

.

61.Give the truth table for a half adder.

Input		Output	
X	Y	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

62.Give the truth table for a half Subtractor.

Input		Output	
X	Y	Borrow(B)	Diffe (D)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

63.From the truth table of a half adder derive the logic equation

$S = X \oplus Y$

$C = X . Y$

64. From the truth table of a half subractor derive the logic equation

$D = X \oplus Y$

$B = X^1 . Y$

65.From the truth table of a full adder derive the logic equation

$S = X \oplus Y \oplus Z$

$C = XY + YZ + XZ$

66.What is code conversion?

If two systems working with different binary codes are to be synchronized in operation, then we need digital circuit which converts one system of codes to the other. The process of conversion is referred to as code conversion.

67.What is code converter?

It is a circuit that makes the two systems compatible even though each uses a different binary code. It is a device that converts binary signals from a source code to its output code. One example is a BCD to Xs3 converter.

68.What do you mean by analyzing a combinational circuit?

The reverse process for implementing a Boolean expression is called as analyzing a combinational circuit. (ie) the available logic diagram is analyzed step by step and finding the Boolean function

69.Give the applications of Demultiplexer.

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i) It finds its application in Data transmission system with error detection.

ii) One simple application is binary to Decimal decoder.

70.Mention the uses of Demultiplexer.

Demultiplexer is used in computers when a same message has to be sent to different receivers. Not only in computers, but any time information from one source can be fed to several places.

71.Give other name for Multiplexer and Demultiplexer.

Multiplexer is other wise called as Data selector.

Demultiplexer is otherwise called as Data distributor.

72.What is the function of the enable input in a Multiplexer?

The function of the enable input in a MUX is to control the operation of the unit.

73.Give the truth table for a full Subtractor.

Input			Output	
X	Y	Z	Borrow (B)	Diffe (D)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

74.Give the truth table for a full adder.

Input			Output	
X	Y	Z	Sum (S)	Carry (C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

75.From the truth table of a full subtractor derive the logic equation

$S = X \oplus Y \oplus Z$

$C = X^1Y + YZ + X^1Z$

76.What is priority encoder?

A priority encoder is an encoder that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

77.Can a decoder function as a Demultiplexer?

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Yes. A decoder with enable can function as a Demultiplexer if the enable line E is taken as a data input line A and B are taken as selection lines.

78.List out the applications of multiplexer?

The various applications of multiplexer are

a. Data routing.
b. Logic function generator.
c. Control sequencer.
d. Parallel-to-serial converter.

79.List out the applications of decoder?

The applications of decoder are

a. Decoders are used in counter system.
b. They are used in analog to digital converter.
c. Decoder outputs can be used to drive a display system.

80.List out the applications of comparators?

The following are the applications of comparator

a. Comparators are used as a part of the address decoding circuitry in computers to select a specific input/output device for the storage of data.
b. They are used to actuate circuitry to drive the physical variable towards the reference value.
c. They are used in control applications.

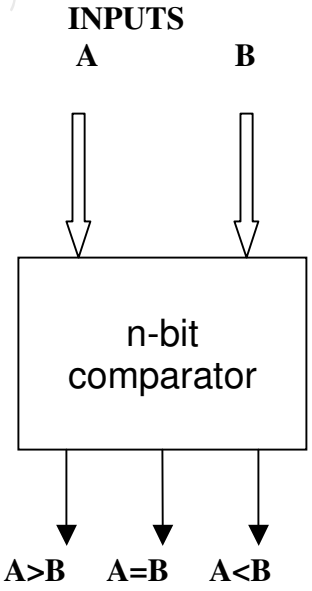
81.What are the applications of seven segment displays?

The seven segment displays are used in

a. LED displays
b. LCD displays

82.What is digital comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.



Block diagram of n-bit comparator

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83. List the types of ROM.

i) Programmable ROM (PROM)
ii) Erasable ROM (EPROM)
iii) Electrically Erasable ROM (EEROM)

84.Differentiate ROM & PLD's

ROM (Read Only Memory)	PLD's (Programmable Logic Array)
1.It is a device that includes both the decoder and the OR gates with in a single IC package	1.It is a device that includes both AND and OR gates with in a single IC package
2.ROM does not full decoding of the variables and does generate all the minterms	2.PLD's does not provide full decoding of the variable and does not generate all the minterms

85.What are the different types of RAM?

The different types of RAM are

a. NMOS RAM (Nitride Metal Oxide Semiconductor RAM)
b. CMOS RAM (Complementary Metal Oxide Semiconductor RAM)
c. Schottky TTL RAM
d. ELL RAM.

86.What are the types of arrays in RAM?

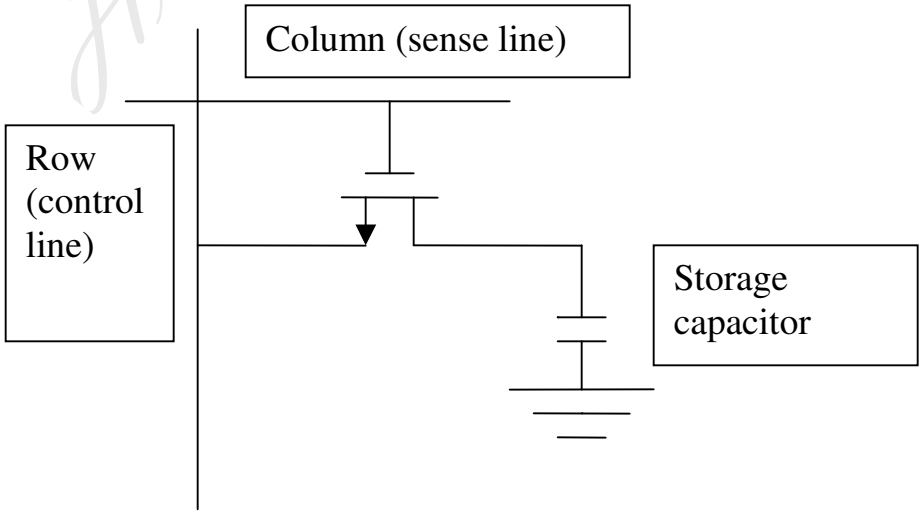
RAM has two type of array namely,

a. Linear array
b. Coincident array

87.Explain DRAM?

The dynamic RAM (DRAM) is an operating mod, which stores the binary information in the form of electric charges on capacitors.

The capacitors are provided inside the chip by MOS transistors.



DRAM cell

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The stored charges on the capacitors tend to discharge with time and the capacitors must be tending to discharge with time and the capacitors must be periodically recharged by refreshing the dynamic memory.

DRAM offers reduced power consumption and larger storage capacity in a single memory chip.

88.Explain SRAM?

Static RAM (SRAM) consists of internal latches that store the binary information. The stored information remains valid as long as the power is applied to the unit.

SRAM is easier to use and has shorter read and write cycle.

The memory capacity of a static RAM varies from 64 bit to 1 mega bit.

89.Differentiate volatile and non-volatile memory?

Volatile memory	Non-volatile memory
They are memory units which lose stored information when power is turned off. E.g. SRAM and DRAM	It retains stored information when power is turned off. E.g. Magnetic disc and ROM

90.What are the terms that determine the size of a PAL?

The size of a PLA is specified by the

a. Number of inputs
b. Number of products terms
c. Number of outputs

91.What are the advantages of RAM?

The advantages of RAM are

a. Non-destructive read out
b. Fast operating speed
c. Low power dissipation
d. Compatibility
e. Economy

92.What is VHDL?

VHDL is a hardware description language that can be used to model a digital system at many level of abstraction, ranging from the algorithmic level to the gate level.

The VHDL language as a combination of the following language.

a. Sequential language
b. Concurrent language
c. Net-list language
d. Timing specification
e. Waveform generation language.

93.What are the features of VHDL?

The features of VHDL are

a. VHDL has powerful constructs.
b. VHDL supports design library.
c. The language is not case sensitive.

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94.Define entity?

Entity gives the specification of input/output signals to external circuitry. An entity is modeled using an entity declaration and at least one architecture body. Entity gives interfacing between device and others peripherals.

95.List out the different elements of entity declaration?

The different elements of entity declaration are:

1. entity_name
2. signal_name
3. mode
4. in:
5. out:
6. input
7. buffer
8. signal_type

96.Give the syntax of entity declaration?

```
ENTITY      entity_name is
PORT (signal_name: mode signal_type;
        signal_names: mode signal_type;
            :
            :
            signal_names: mode signal_type;
END entity_name;
```

97.What do you meant by concurrent statement?

Architecture contains only concurrent statements. It specifies behavior, functionality, interconnections or relationship between inputs and outputs.

98.What are operates used in VDHL language?

There are different types of operators used in VHDL language

Logical operators : AND, OR, NOT, XOR, etc.,
Relational operator : equal to, <less than etc.,
Shift operators : SLL- Shift Left Logical,
ROR- Rotate Right Logical etc.,
Arithmetic operators: Addition, subtraction etc.,
Miscellaneous operators: <= assign to etc.,

99.Define VHDL package?

A VHDL, package is a file containing definitions of objects which can be used in other programs. A package may include objects such as signals, type, constant, function, procedure and component declarations

100.What is meant by memory decoding?

The memory IC used in a digital system is selected or enabled only for the range of addresses assigned to it .

101.What is access and cycle time?

The access time of the memory is the time to select word and read it. The cycle time of a memory is a time required to complete a write operation.

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102.What is sequential circuit?

Sequential circuit is a broad category of digital circuit whose logic states depend on a specified time sequence. A sequential circuit consists of a combinational circuit to which memory elements are connected to form a feedback path.

103.List the classifications of sequential circuit.

i) Synchronous sequential circuit.
ii) Asynchronous sequential circuit.

104.what is Synchronous sequential circuit?

A Synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signal at discrete instants of time.

105.What is clocked sequential circuits?

Synchronous sequential circuit that use clock pulses in the inputs of memory elements are called clocked sequential circuit. One advantage as that they don't cause instability problems.

106.What is called latch?

Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.

107.List different types of flip-flops.

i) SR flip-flop
ii) Clocked RS flip-flop
iii) D flip-flop
iv) T flip-flop
v) JK flip-flop
vi) JK master slave flip-flop

108.What do you mean by triggering of flip-flop.

The state of a flip-flop is switched by a momentary change in the input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop

109.What is an excitation table?

During the design process we usually know the transition from present state to next state and wish to find the flip-flop input conditions that will cause the required transition. A table which lists the required inputs for a given chance of state is called an excitation table.

110.Give the excitation table of a JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

111.Give the excitation table of a SR flip-flop

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Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

112.Give the excitation table of a T flip-flop

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

113.Give the excitation table of a D flip-flop

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	0
1	1	1

114.What is a characteristic table?

A characteristic table defines the logical property of the flip-flop and completely characteristic its operation.

115.Give the characteristic equation of a SR flip-flop.

$Q(t+1)=S+R^1Q$

116.Give the characteristic equation of a D flip-flop.

$Q(t+1)=D$

117.Give the characteristic equation of a JK flip-flop.

$Q(t+1)=JQ^1+K^1Q$

118.Give the characteristic equation of a T flip-flop.

$Q(t+1)=TQ^1+T^1Q$

119.What is the difference between truth table and excitation table.

i) **An excitation table is a table that lists the required inputs for a given change of state.**

ii) **A truth table is a table indicating the output of a logic circuit for various input states.**

120.What is counter?

A counter is used to count pulse and give the output in binary form.

121.What is synchronous counter?

In a synchronous counter, the clock pulse is applied simultaneously to all flip-flops. The output of the flip-flops change state at the same instant. The speed of operation is high compared to an asynchronous counter

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122.What is Asynchronous counter?

In a Asynchronous counter, the clock pulse is applied to the first flip-flops. The change of state in the output of this flip-flop serves as a clock pulse to the next flip-flop and so on. Here all the flip-flops do not change state at the same instant and hence speed is less.

123.What is the difference between synchronous and asynchronous counter?

Sl.No.	Synchronous counter	Asynchronous counter
1.	Clock pulse is applied simultaneously	Clock pulse is applied to the first flip-flop, the change of output is given as clock to next flip-flop
2.	Speed of operation is high	Speed of operation is low.

124.Name the different types of counter.

a) Synchronous counter
b) Asynchronous counter
i) Up counter
ii) Down counter
iii) Modulo – N counter
iv) Up/Down counter

125.What is up counter?

A counter that increments the output by one binary number each time a clock pulse is applied.

126.What is down counter?

A counter that decrements the output by one binary number each time a clock pulse is applied.

127.What is up/down counter?

A counter, which is capable of operating as an up counter or down counter, depending on a control lead.

128.What is a ripple counter?

A ripple counter is nothing but an asynchronous counter, in which the output of the flip-flop change state like a ripple in water.

129.What are the uses of a counter?

i) The digital clock
ii) Auto parking control
iii) Parallel to serial data conversion.

130.What is meant by modulus of a counter?

By the term modulus of a counter we say it is the number of states through which a counter can progress.

131.what is meant by natural count of a counter?

By the term natural count of a counter we say that the maximum number of states through which a counter can progress.

132.A ripple counter is a ---------- sequential counter.

Ans: Synchronous.

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133.What is a modulo counter?

A counter that counts from 0 to T is called as modulo counter.

134.A counter that counts from to T is called a modulo counter. True or False.

Ans: True

135.The number of flip-flops required for modulo-18 counter is -------

Ans: five.

136.Form the truth table for 3-bit binary down counter.

Clk	Q2	Q1	Q0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
1	1	1	1

137.What is a ring counter?

A counter formed by circulating a 'bit' in a shift register whose serial output has been connected to its serial input.

138.What is BCD counter?

A BCD counter counts in binary coded decimal from 0000 to 1001 and back to 0000. Because of the return to 0000 after a count of 1001, a BCD counter does not have a regular pattern as in a straight binary counter.

139. What are the uses of a ring counter?

i) Control section of a digital system.

ii) Controlling events, which occur in strict time sequence.

140.What is a register?

Memory elements capable of storing one binary word. It consists of a group of flip-flops, which store the binary information.

141.What is Johnson counter?

It is a ring counter in which the inverted output is fed into the input. It is also know as a twisted ring counter.

142. What is a shift register?

In digital circuits, datas are needed to be moved into a register (shift in) or moved out of a register (shift out). A group of flip-flops having either or both of these facilities is called a shift register.

143. What is serial shifting?

In a shift register, if the data is moved 1 bit at a time in a serial fashion, then the technique is called serial shifting.

144. What is parallel shifting?

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In a shift register all the data are moved simultaneously and then the technique is called parallel shifting.

145. Write the uses of a shift register.

i) Temporary data storage
ii) Bit manipulations.

146. What is a cycle counter?

A cycle counter is a counter that outputs a stated number of counts and then stops.

147. Define state of sequential circuit?

The binary information stored in the memory elements at any given time defines the "state" of sequential circuits.

148. Define state diagram.

A graphical representation of a state table is called a state diagram.

149. What is the use of state diagram?

i) Behavior of a state machine can be analyzed rapidly.
ii) It can be used to design a machine from a set of specification.

150. What is state table?

A table, which consists time sequence of inputs, outputs and flip-flop states, is called state table. Generally it consists of three section present state, next state and output.

151. What is a state equation?

A state equation also called, as an application equation is an algebraic expression that specifies the condition for a flip-flop state transition. The left side of the equation denotes the next state of the flip-flop and the right side; a Boolean function specifies the present state.

152.What is meant by race around condition?

In JK flip-flop output is fed back to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

153. How many bits would be required for the product register if the multiplier has 6 bits and the multiplicand has 8 bits?

The product register is 14-bit width with extra bit at the left end indicating a temporary storage for any carry, which is generated when the multiplicand is added to the accumulator.

154. What is SM chart?

Just as flow charts are useful in software design, flow charts are useful in the hardware design of digital systems. These flow charts are called as State Machine Flow Charts or SM charts. SM charts are also called as ASMC (Algorithmic State machine chart). ASM chart describes the sequential operation in a digital system.

155. What are the three principal components of SM charts?

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The 3 principal components of SM charts are state box, decision box & Conditional output box.

156. What is decision box?

A diamond shaped symbol with true or false branches represents a decision box. The condition placed in the box is a Boolean expression that is evaluated to determine which branch to take in SM chart.

157. What is link path? How many entrance paths & exit paths are there in SM block?

A path through an SM block from entrance to exit is referred to as link path. An SM block has one entrance and exit path.

158. Differentiate ASM chart and conventional flow chart?

A conventional Flow chart describes the sequence of procedural steps and decision paths for an algorithm without concern for their time relationship.

The ASM chart describes the sequence of events as well as the timing relationships between the states of a sequential controller and the events that occur while going from one state to the next.

159. What is flow table?

During the design of synchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values. Such table is called Flow table.

160. What is primitive flow table?

A flow table is called Primitive flow table because it has only one stable state in each row.

161. Define race condition.

A race condition is said to exist in a synchronous sequential circuit when two or more binary state variables change, the race is called non-critical race.

162. Define critical & non-critical race with example.

The final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called non-critical race.

The final stable state that the circuit reaches depends on the order in which the state variables change, the race is called critical race.

163. How can a race be avoided?

Races can be avoided by directing the circuit through intermediate unstable states with a unique state – variable change.

164. Define cycle and merging?

When *a* circuit goes through a u*n*ique sequence of unstable states, *i*t is said to have a cyc*l*e.

The *g*rouping of stab*l*e states from s*e*parate rows into o*n*e common row is called merging.

165. Give state – reduction procedure.

The state – reduction procedure for co*m*pletely specified st*a*te tables is base*d* on t*h*e algorithm that two state*s* in a state table can be combined in to one if they can be shown to be equi*v*a*l*e*n*t.

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166. Define hazards.

Hazards are unwanted switching transients that may appear at the output of a circuit because different paths exhibit different propagation delays.

167. Does Hazard occur in sequential circuit? If so what is the problem caused?

Yes, Hazards occur in sequential circuit that is Asynchronous sequential circuit. It may result in a transition to a wrong state.

168. Give the procedural steps for determining the compatibles used for the purpose of merging a flow table.

The purpose that must be applied in order to find a suitable group of compatibles for the purpose of merging a flow table can be divided into 3 procedural steps.

- **i. Determine all compatible pairs by using the implication table.**
- **ii. Find the maximal compatibles using a Merger diagram**
- **iii. Find a minimal collection of compatibles that covers all the states and is closed.**

169. What are the types of hazards?

The 3 types of hazards are 1) Static – 0 hazards
2) Static – 1 hazard
3) Dynamic hazards

170.What is mealy and Moore circuit?

Mealy circuit is a network where the output is a function of both present state and input.

Moore circuit is a network where the output is function of only present state.

171.Differentiate Moore circuit and Mealy circuit?

Moore circuit	Mealy circuit
a. It is output is a function of present state only. b. Input changes do not affect the output. c. Moore circuit requires more number of states for implementing same function.	a. It is output is a function of present state as well as the present input. b. Input changes may affect the output of the circuit. c. It requires less numbers of states for implementing same function.

172. How can the hazards in combinational circuit be removed?

Hazards in the combinational circuits can be removed by covering any two min terms that may produce a hazard with a product term common to both. The removal of hazards requires the addition of redundant gates to the circuit.

173. How does an essential hazard occur?

An essential hazard occurs due to unequal delays along two or more paths that originate from the same input. An excessive delay through an inverter circuit in comparison to the delay associated with the feedback path causes essential hazard.

174.what is Timing diagram?

Timing diagrams are frequently used in the analysis of sequential network. These diagrams show various signals in the network as a function of time.

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175.What is setup and hold time?

The definite time in which the input must be maintained at a constant value prior to the application of the pulse is setup time

The definite time is which the input must not chance after the application of the positive or negative going transition of the pulse based on the triggering of the pulse.

176.Define bit time and word time.

The time interval between clock pulses is called bit time.

The time required to shift the entire contents of a shift register is called word time.

177.What is bi-directional shift register and unidirectional shift register?

A register capable of shifting both right and left is called bi-directional shift register.

A register capable of shifting only one direction is called unidirectional shift register.

178.Define equivalent state.

If a state machine is started from either of two states and identical output sequences are generated from every possible set of sequences, then the two states are said to be equivalent.

179.If a shift register can be operated in all possible ways then it is called as----------

Ans: Univerasal register: It can be operated in all possible modes with bi-directional shift facility.

180.What is gate delay?

If the change in output is delayed by a time ε with respect to the input. We say that the gate has a propagation delay of ε. Normally propagation delay for 0 to 1 output (ε1) may be different than the delay for 1 to 0 changes (ε2).

181.Define state reduction algorithm.

State reduction algorithm is stated as "Two states are said to be equivalent if, for each member of the set of inputs they give the same output and send the circuit either to the same state or to an equivalent state. When two states are equivalent, one of them can be removed without altering the input-output relation.

182.What is meant by level triggering?

In level triggering the output of the flip-flop changes state or responds only when the clock pulse is present.

183.Write the uses of a shift register.

i) Temporary data storage.

ii) Bit manipulations.

184. What is meant by flow table?

During the design of asynchronous sequential circuits, it is more convenient to name the states by letter symbols without making specific reference to their binary values. Such a table is called a flow table.

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185. What are the problems involved in asynchronous circuits?

The asynchronous sequential circuits have three problems namely,

a. Cycles
b. Races
c. Hazards

186. Define cycles?

If an input change includes a feedback transition through more than unstable state then such a situation is called a cycle.

187. Define primitive flow table?

A primitive flow table is a flow table with only one stable total state in each row. Remember that a total state consists of the internal state combined with the input.

188. Define merging?

The primitive flow table has only one stable state in each row. The table can be reduced to a smaller numbers of rows if two or more stable states are placed in the same row of the flow table. The grouping of stable states from separate rows into one common row is called merging.

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UNIT I

1. Simplify the following Boolean function by using Tabulation method

   $F(w, x, y, z) = \Sigma(0,1,2,8,10,11,14,15)$

   - Determination of Prime Implicants
   - Selection of prime Implicants

2. Simplify the following Boolean functions by using K'Map in SOP & POS.

   $F(w, x, y, z) = \Sigma(1,3,4,6,9,11,12,14)$

   - Find the Number of variable map
   - Draw the Map
   - Simplification of SOP & POS

3. Simplify the following Boolean functions by using K'Map in SOP & POS.

   $F(w, x, y, z) = \Sigma(1,3,7,11,15) + d(0,2,5)$

   - Find the Number of variable map
   - Don't care treat as variable X.
   - Draw the Map
   - Simplification of SOP & POS

4. Reduce the given expression.

   $[(AB)^1 + A^1 + AB]^1$

   - Reduce the expression using Boolean algebra Laws and theorems

5. Reduce the given function minimum number of literals.

   $(ABC)^1 + A^1) + AC$

   - Reduce the expression using Boolean algebra Laws and theorems

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UNIT II

1. Design a combinational logic circuit to convert the Gray code into Binary code

   - Truth table
   - K'Map Simplification
   - Draw the Logic Diagram

2. Draw the truth table and logic diagram for full-Adder

   - Truth table
   - K'Map Simplification
   - Draw the Logic Diagram

3. Draw the truth table and logic diagram for full-Subtractor

   - Truth table
   - K'Map Simplification
   - Draw the Logic Diagram

4. Explain Binary parallel adder.

   - Explanation
   - Logic diagram

5. Design a combinational logic circuit to convert the BCD to Binary code

   - Truth table
   - K'Map Simplification
   - Draw the Logic Diagram

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UNIT III

1. Implement the following function using PLA.

   A (x, y, z) = Σm (1, 2, 4, 6)
   B (x, y, z) = Σm (0, 1, 6, 7)
   C (x, y, z) = Σm (2, 6)

   - K'Map Simplification
   - PLA table
   - PLA Logic Diagram

2. Implement the following function using PAL.

   W (A, B, C, D) = Σm (2, 12, 13)
   X (A, B, C, D) = Σm (7, 8, 9, 10, 11, 12, 13, 14, 15)
   Y (A, B, C, D) = Σm (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)
   Z (A, B, C, D) = Σm (1, 2, 8, 12, 13)

   - K'Map Simplification
   - PAL Logic diagram

3.Implement the given function using multiplexer

   - Implementation table
   - Multiplexer Implementation

4. Explain about Encoder and Decoder?

   - Definition
   - Truth table
   - Logic Diagram

5. Explain about 4 bit Magnitude comparator?

   - Explanation
   - Logic Diagram

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UNIT IV

1. Design a counter with the following repeated binary sequence: **0, 1, 2, 3, 4, 5, 6.** use JK Flip-flop.
   - State diagram
   - Excitation State table
   - K'Map Simplification
   - Logic diagram

2. Describe the operation of SR flip-flop
   - Logic Diagram
   - Graphical Symbol
   - Characteristics table
   - Characteristics equation
   - Excitation Table

3. Design a sequential circuit using JK flip-flop for the following state table [use state diagram]

Present state	Next state		Output	
AB	X=0	X=1	X=0	X=1
00	00	11	1	0
01	01	11	1	1
10	01	00	1	0
11	11	10	0	0

   - State Diagram
   - Excitation state table
   - K'Map simplification
   - Logic Diagram

4. The count has a repeated sequence of six states, with flip flops B and C repeating the binary count 00, 01, 10 while flip flop A alternates between 0 and 1 every three counts. Designs with JK flip-flop
   - State diagram
   - Excitation State table
   - K'Map Simplification
   - Logic diagram

5. Design a 3-bit T flip-flop counter
   - State diagram
   - Excitation State table
   - K'Map Simplification
   - Logic diagram

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UNIT V

1. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input.

   - State Table
   - Primitive Flow Table
   - Formal Reduction (Implication Method)
   - Merging
   - Reduced Table
   - K'Map Simplification
   - Logic Diagram

2. Give hazard free relation for the following Boolean function.

   $F(A, B, C, D) = \Sigma m (0, 2, 6, 7, 8, 10, 12)$

   - K'Map simplification
   - Create Hazard free link

3. Explain about Hazards?

   - Explain Static Hazard
   - Explain Dynamic Hazard

4. Explain about Races?

   - Explain Critical Race
   - Explain Non-Critical Race

5. Design T Flip flop from Asynchronous Sequential circuit?

   - State Table
   - Primitive Flow Table
   - Formal Reduction (Implication Method)
   - Merging
   - Reduced Table
   - K'Map Simplification
   - Logic Diagram

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