B. E. VIIth Semester (Compt. Science) Engg. Examination

ADVANCED COMPT. ARCHITECTURE

Paper–CSE-401-C

Time allowed : 3 hours *Maximum Marks : 100*

***Note** : Attempt any **five** questions.*

1. (a) Discuss the relative advantages of update and invalidate protocols for bus based shared memory multiprocessors. 10

   (b) Discuss the relative advantages of update and invalidate protocols for multi-node switched shared memory multiprocessors. 10

2. Discuss in brief

   (a) Multiple-issue machine 10

   (b) Out of order execution. 10

3. (a) When memory is implemented using DRAM organised as $2^k \times 4$, the failure of a single chip can result in error of up to four bits. Devise an error correction scheme for device failure. Detail the scheme for m = 16. 10

   (b) For a copyback cache (CBWA) and W = 0.5 using memory system T_s = 200 ns, T_c = 100 ns, n=8, T_{bus} = 25, L = 16 compute $T_{m,miss}$, $T_{c,miss}$, T_{busy} for

   (i) Unbuffered line transfers starting at line address.

(ii) Write buffer, line transfers starting at line address.

(iii) Buffered transfers with wraparound load. 10

4. (a) Discuss various write policies for caches. 8

(b) What do you mean by cache-mapping ? Explain the set associative mapping scheme for cache with the help of a diagram. 12

5. (a) Differentiate between static and dynamic pipeline. 6

(b) Discuss the following :

(i) Branch elimination 7

(ii) Branch prediction strategies. 7

6. (a) Discuss the relative advantages and disadvantages of fixed and floating point representation of numbers. 10

(b) Explain the virtual to real address mapping. Give an example to support your answers. 10

7. (a) Describe various phases in a processor design project. 10

(b) Discuss the role of registers, evaluation stacks and data buffers in processor evaluation. 10

8. Write short notes on :

(a) Process Management 10

(b) Data Categories. 10