Printed Pages : 4   **MCA – 206**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1471   Roll No. ☐☐☐☐☐☐☐☐☐☐

M. C. A.

(SEM. II) EXAMINATION, 2006-07

COMPUTER ARCHITECTURE &
MICROPROCESSOR

Time : 3 Hours]   *[Total Marks : 100*

Note :   (1)   *Attempt **all** questions.*

(2)   *All questions carry **equal** marks.*

1   Attempt any **two** parts of the following :

(a)   Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

(b)   (i)   Determine the number of pipe clock cycles that it takes to process 200 tasks in a six-segment pipeline.

(ii)   A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks.

(c)   Explain the following :

(i)   Serial versus parallel processing

(ii)   Parallelism versus pipelining.

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2   Attempt any **two** parts of the following:

(a)   Explain two techniques for enhancing the performance of computers with multiple execution pipeine.

(b)   The following overlayed reservation table corresponds to a two-function (A,B) pipeline.

	t_0	t_1	t_2	t_3	t_4
S_1	A	B		A	B
S_2		A		B	A
S_3	B		A B		

(i)   List all four cross forbidden lists of latencies and corresponding combined cross-collision matrices.

(ii) Draw the state diagram for the two functional pipeline.

(c)   Suppose that scalar operations take 10 times longer to execute per result than vector operations. Given a program which is originally written in scalar code:

(i)   What are the percentage of the code needed to be vectorized in order to achieve the speed up factors of 2,4 and 6 respectively ?

(ii) Suppose the program contains 15% of code that cannot be vectorized such as sequential I/o operations. Now repeat part (i) for the remaining code to achieve the three speed up factors.

3   Attempt any **two** parts of the following :

(a)   In case of SIMD inter connection networks, explain the various static interconnection network topologies.

(b)   Write down an O (n^2) algorithm and an O $(n \log_2 n)$ algorithm for matrix multiplication and explain it.

(c) Prove or disprove that the Omega network can perform any shift permutation in one pass. The shift permutation is defined as follows: given $N=2^n$ inputs, a shift permutation is either a circular left shift or a circular right shift of k positions, where $0 \ k < N$.

4   Attempt any **two** parts of the following:

(a) Explain the functional structures of Loosely coupled Microprocessors and Tighty coupled Microprocessors.

(b) Explain the following:

   (i) List scheduling algorithm

   (ii) Coffman and Graham algorithm.

(c) (i) What are the major design issues towards the practical realization of a data flow computer ?

   (ii) What are the data flow graphs? Explain with the help of an example.

5   Attempt any **four** of the following :

(a) What are tri-state devices and why are they essential in a bus-oriented system?

(b) List three improved features of the 8085 over the 8080A microprocessor.

(c) Define: Instruction cycle, machine cycle and T-state.

(d) Write a program to :

   (i) Clear the accumulator

   (ii) Add 47H (use ADI instruction)

   (iii) Subtract-92H

   (iv) Add 64H

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(v) Display the result after subtracting 92H and after ading 64H.

Specify the answers you would expect at the output ports.

(e) Add the following five data bytes stored in memory locations starting 2060H and display the sum (the sum if less than FF. Use register B to store the partial sum). Write the program without using ADD M.

(f) Write a 20 ms time delay subroutine using register pair BC. Clear the Z flag without affecting any other flags in the flag register, and returns to the main program.

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