ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2008

VLSI CIRCUITS & SYSTEMS

SEMESTER – 6

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) Pseudo NMOS logic provides which of the following advantages ?

a) Static power dissipation is less compared to CMOS logic

b) It is much faster compared to other logics

c) It requires less no. of transistors compared to CMOS logic

d) It is more noise immune. ☐

ii) Frequency Compensation for an OP-AMP can be achieved by

a) increasing gain b) minimizing overall phase shift

c) adding a zero d) none of these. ☐

iii) Among the given OP-AMP topologies which one has the highest output swing ?

a) Telescopic b) Folded Cascaded

c) Two Stage d) Gain Boosted. ☐

iv) Typical value of subthreshold slope is

a) 80 mV/decade b) 60 mV/decade

c) 40 mV/decade d) 90 mV/decade. ☐

v) Slant in ($I_D - V_{ds}$) occurs due to

a) body effect b) velocity saturation

c) channel length modulation d) mobility degradation.

vi) The unit for ($\mu_n C_{ox}$) is

a) A/V^2 b) V^{-1}

c) ohm d) $(\text{ohm})^{-1}$

e) No unit.

vii) To implement the Boolean function $F = \overline{A(B + CD)}$ using static CMOS design, number of transistors required is

a) 4 b) 8

c) 6 d) 12.

viii) A logic gate has V_{OH} = 5V, V_{OL} = 0·2V, V_{IH} = 2·5V and V_{IL} = 0·8 V. The noise margins are

a) 0·6 V and 2·5 V b) 2·3 V and 4·2 V

c) 1·7 V and 2·3 V d) 1·7 V and 4·8 V.

ix) DRAM is widely used because

a) refreshing operation is not needed

b) of low cost and high density

c) of low power consumption

d) of high speed.

x) The model parameter LAMDA (λ) in a MOS structure stands for

a) Flicker noise coeffficient

b) Transit time

c) Channel length modulation

d) Transconductance.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Design the following circuits using Transmission Gates : $2 \times 2\frac{1}{2}$

   a) D Flip-flop

   b) 2 input XOR Gate.

3. Explain how a combination of swithches and capacitors can be used to emulate a resistor. 5

4. Design a current sink of 30 μA assuming the mirror transistor current is 10 μA. Given $V_{DD} = -V_{SS} = 2{\cdot}5$ V, $V_{GS} = 1{\cdot}2$ V and W/L ratio for the mirror transistor as 15/5. 5

5. Explain why NOR Gates are preferred for NMOS circuits while NAND Gates are preferred for static CMOS circuits. 5

6. Describe the following pheomena in MOS structure : $2 \times 2\frac{1}{2}$

   a) Velocity saturation

   b) Channel length modulation.

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) Describe in detail Lamda-based design rule for layout design.

   b) What is stick diagram ? Mention its use.

   c) What do you mean by active layer and poly layer in CMOS process ?

   d) Write down the difference between twin-tub process and *p*-well process.

   $6 + 3 + 3 + 3$

8. a) Draw the circuit diagram of dual slope A/D converter and explain its operation.

   b) What is a phase locked loop ? Mention two uses of phase locked loop.

   c) Realize an active LPF of cut-off frequency 10 kHz and gain 10. $6 + 5 + 4$

9. a) Draw the layout of a CMOS inverter (not to scale). Explain your drawing conventions.

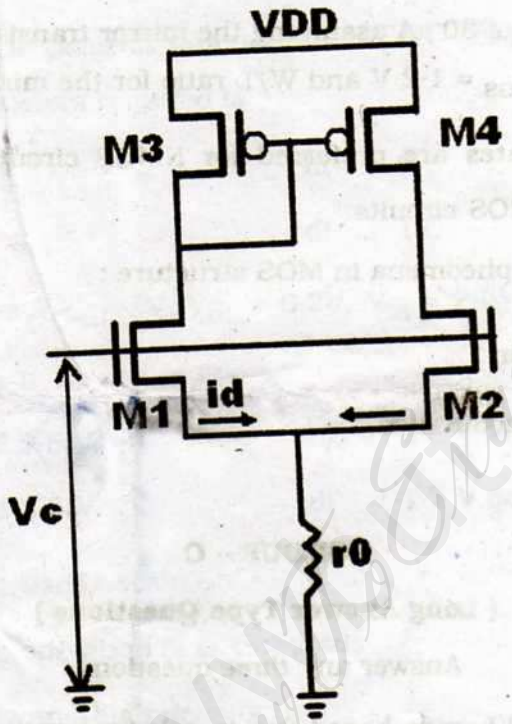
b) Design a static CMOS circuit to implement the Boolean function

$F = \bar{D} \cdot \bar{E} \cdot \bar{A} + \bar{B} \cdot \bar{C}$.

c) Draw the circuit of a CMOS full adder circuit and explain its operation. 5 + 5 + 5

10. a) Explain with a circuit diagram, operation of a differential amplifier.

b) What is CMRR ? Determine CMRR of the following circuit.



6 + (3 + 6)

11. a) Why is reference voltage required in IC ? What are the criteria for a good reference voltage source in VLSI circuit ?

b) Explain the operation of a band gap voltage reference source in a VLSI circuit.

c) Explain briefly difficult stages of an operational amplifier with the help of a block diagram. (2 + 2) + 7 + 4

END