



**ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2009**

**VLSI CIRCUITS & SYSTEMS**

**SEMESTER - 6**

Time : 3 Hours ]

[ Full Marks : 70

**GROUP - A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) What is another name of D. Gzaski chart ?

- a) Y Chart
- b) Smith Chart
- c) Z Chart
- d) Log Chart.

ii) Channel-less Gate array is a sub-type of

- a) FPGA
- b) PLD
- c) ASIC
- d) None of these.

iii) Minimum number of transistors required to implement  $F = ABC + DE + F$  is

- a) 5
- b) 6
- c) 7
- d) none of these.

iv) The output of physical design is

- a) Circuit diagram
- b) Mask
- c) Lay-out
- d) RTL.

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- v) DRAM is widely used because
- a) refreshing operation is not needed
  - b) of low cost and high density
  - c) of low power consumption
  - d) of high speed.

vi) Data refresh operation is needed in

- a) DRAM
- b) Flash
- c) SRAM
- d) FRAM.

vii) For a symmetrical CMOS inverter the relation between aspect ratio of NMOS and PMOS is

- a)  $(W/L)_p = (W/L)_n$
- b)  $(W/L)_p = 2.5 (W/L)_n$
- c)  $(W/L)_n = 2.5 (W/L)_p$
- d)  $(W/L)_n = 5 (W/L)_p$ .

viii) Frequency compensation of Op-Amp using MOS technology is done by

- a) decreasing the number of stages
- b) minimizing the number of poles in single path
- c) achieving low voltage gain
- d) all of these.

ix) A BJT is considered as Open Switch ( or OFF ) when

- a) both junctions are forward biased
- b) EBJ is forward and CBJ is reverse
- c) both junctions are reverse biased
- d) EBJ is reverse and CBJ is forward.

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x) Hierarchical decomposition of a large system in VLSI design is called

- a) modularity
- b) regularity
- c) locality
- d) none of these.

xi) Which of the following is not a part of FPGA ?

- a) CLB
- b) I/O Block
- c) Vertical routing channel
- d) FSM.

xii) The quantisation noise of a DAC having  $N$  number of bits is

- a) directly proportional to  $2^N$
- b) directly proportional to  $2^{N-1}$
- c) inversely proportional to  $2^N$
- d) inversely proportional to  $2^{N-1}$ .

**GROUP - B**

**( Short Answer Type Questions )**

Answer any *three* of the following.

3 × 5 = 15

2. What is MOSFET scaling ? What is the need of scaling ? Compare various types of scaling. 1 + 2 + 2

3. Explain the following phenomenon in an MOS structure : 3 + 2

- a) Channel length modulation
- b) Pinch-off.

4. a) What do you mean by VHDL ? Why is it required in VLSI circuit simulation ? 1 + 1

b) Derive saturation current in an  $n$ -MOS transistor. 3

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5. a) What is current mirror ?  
 b) With circuit diagram explain the operation of an MOS current mirror. 1 + 4
6. Draw the layout and schematic diagram of a 2-input static CMOS NOR Gate and identify the corresponding components in the two drawings. 1 + 1 + 3

### GROUP - C

#### ( Long Answer Type Questions )

Answer any three of the following.

3 × 15 = 45

7. a) What is Y cycle in VLSI ? Explain VLSI design cycle in detail. 2 + 6  
 b) What do you mean by standard cell design ? How does it differ from gate array design ? 2 + 3  
 c) What is top-down and bottom-up design in VLSI ? 2
8. a) Design a static CMOS circuit to implement the Boolean function :  

$$F = AB + AB'C + A'C'$$
 7  
 b) Draw the CMOS half adder circuit and explain its operation. 5  
 c) Explain why NMOS is preferred for pull-down network and PMOS is preferred for pull-up network. 3
9. a) Design the following circuit using PAL, PLA and ROM :  

$$Y_1 = AB + A'C + ABC', Y_2 = AB'C, Y_3 = BC + ABC'$$
 6  
 b) Design a master-slave D flip-flop. Describe its operation. 3  
 c) Describe the read and write operation of a six transistor SRAM cell. 6

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10. a) Explain lambda ( $\lambda$ ) design rules in VLSI. 4
- b) Compare the advantage of lambda design rule over micron rule. 3
- c) What is CMOS twin tub process ? Explain. 3
- d) Find out an expression for dynamic power dissipation in CMOS. 3
- e) What are the properties of VLSI interconnects ? 2
11. a) Discuss the merits and demerits of Flash ADC. Find resolution for a DAC if the output voltage is desired to change in 1mV increments while using a reference voltage of 5V ? 2 + 3
- b) How can a MOS device be used as a voltage reference ? 5
- c) What do you mean by hierarchy, regularity, modularity & locality of any ASIC design. 5

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END

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