



**ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2009**  
**ADVANCED COMPUTER ARCHITECTURE**  
**SEMESTER - 4**

Time : 3 Hours ]

[ Full Marks : 70

**GROUP - A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for the following :

10 × 1 = 10

i) The vector stride value is required

- a) to deal with the length of vectors
- b) to find the parallelism in vectors
- c) to access the elements in multi-dimensional vectors
- d) to execute vector instruction.

ii) The performance of a pipelined processor suffers if

- a) the pipeline stages have different delays
- b) consecutive instructions are dependent on each other
- c) the pipeline stages share hardware resources
- d) all of these.

iii) Consider the cache memory with access time 40 ns has the hit ratio of 80%. The regular memory has an access time of 100 ns. What is the effective access time for CPU to access memory ?

- a) 52 ns
- b) 60 ns
- c) 70 ns
- d) 80 ns.

4641 (16/06)



- iv) What is a main advantage of classical vector systems ( VS ) compared to RISC based systems ( RS ) ?
- a) VS have significantly higher memory bandwidth than RS
  - b) VS have higher clock rate than RS
  - c) VS are more parallel than RS
  - d) None of these.
- v) Associative memory is a
- a) pointer addressable memory
  - b) very cheap memory
  - c) content addressable memory
  - d) slow memory.
- vi) The principle of locality justifies the use of
- a) interrupts
  - b) polling
  - c) DMA
  - d) cache memory.
- vii) How many address bits are required for a  $512 \times 4$  memory ?
- a) 512
  - b) 4
  - c) 9
  - d)  $A_0 - A_8$ .
- viii) The division of stages of a pipeline into sub-stages is the basis for
- a) pipelining
  - b) super-pipelining
  - c) superscalar
  - d) VLIW processor.

**4841 (16/06)**



ix) What will be the speed up for a four stage linear pipeline when the number of instruction  $n = 64$  ?

- a) 4.5
- b) 7.1
- c) 6.5
- d) None of these.

x) Dynamic pipeline allows

- a) multiple function to evaluate
- b) only streamline connection
- c) perform fixed function
- d) none of these.

**GROUP - B**

**( Short Answer Type Questions )**

Answer any three of the following questions.

3 x 5 = 15

2. Consider the pipelined execution of these instructions :

- DADD                    R1, R2, R3
- DSUB                    R4, R1, R5
- AND                     R6, R1, R7
- OR                        R8, R1, R9
- XOR                      R10, R1, R11

Explain how the above execution may generate a data hazard and describe a way to minimize the data hazard stalls using forwarding. Modify the above example to show a case where forwarding may not work.

**4641 (16/06)**



3. Consider a computer where the clock per instruction ( CPI ) is 1.0 when all memory accesses hit ( no memory stalls ) in the cache. Assume each clock cycle is 2 ns. The only data accesses are loads and stores, and these total 50% of the instructions. Assume the following formula for calculating execution time :

CPU execution time = ( CPU clock cycles + Memory stall cycles ) × Clock cycle time.

For a program consisting of 100 instructions :

- Calculate the CPU execution time assuming there are no misses.
- Calculate the CPU execution time considering the miss penalty is 25 clock cycles and the miss rate is 2%.

Discuss the difference between write through and write back cache policies.

4. Assume the performance of 1-word wide primary memory organization is

- 4 clock cycles to send the address
- 56 clock cycles for the access time per word
- 4 clock cycles to send a word of data

Given a cache block of 4 words, and that a word is 8 bytes, calculate the miss penalty and the effective memory bandwidth.

Re-compute the miss penalty and the memory bandwidth assuming we have

- Main memory width of 2 words
- Main memory width of 4 words
- Interleaved main memory with 4 banks with each bank 1-word wide.

5. Explain the concept of strip mining used in vector processors. Why do vector processors use memory banks ?

6. Discuss Flynn's classification of parallel computers.

4641 (16/06)



**GROUP - C**

**( Long Answer Type Questions )**

Answer any three of the following questions.

3 × 15 = 45

7. a) Design an arithmetic unit with variable  $S$  and 2  $n$ -bit data inputs  $A$  and  $B$ . The circuit generates following arithmetic operations in conjunction with carry in  $C_{in}$ .

Draw the logic diagram.

$S$	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$	$D = A - 1$
1	$D = A - 1$	$D = A + B' + 1$

b) What is floating point arithmetic operation ? Explain all ( addition, difference, multiplication, division ) operations with example.

c) What are logical address and physical address ? If segment no. is 8, page no. is 04, word no. is 40. Segment no. 8 hold 30 and page no. 30 hold 019, what will be corresponding physical address ? For answer figure is essential. 5 + 5 + 5

8. a) What is I/O interface ?

b) What are I/O vs. Memory Bus and Isolated vs. Memory-Mapped I/O ?

c) What are the different mechanisms of Asynchronous Data Transfer ? Explain in brief.

d) Explain DMA working principle. 2 + 3 + 5 + 5

9. a) What are the different pipeline hazards and what are the remedies ?

b) What is Vector array processor ? Explain with example.

c) Describe Harvard architecture. 5 + 5 + 5

**4641 (16/06)**



10. a) Apply Booth's algorithm to multiply the two numbers + 11 and - 12.
- b) What is the limitation of direct mapping method ? Explain with example how it can be improved in set-associative mapping.
- c) Use 8-bit 2's complement integer to perform  $- 43 + (- 13)$ .
- d) What is a tri-state buffer ? Design a common bus system using tri-state buffers for two registers of 4-bits each.
- e) What is serial adder ? Discuss it briefly with diagram.  $3 + 4 + 3 + 3 + 2$
11. a) What are the different methods for control unit design ? Explain.
- b) Write down the different addressing modes with examples.
- c) What do you mean by pipeline processing ?
- d) What are instruction pipeline and arithmetic pipeline ?
- e) Find 2's complement of  $(1AB)_{16}$  represented in 16 bit format.  $4 + 6 + 2 + 2 + 1$

---

END

4841 (16/08)