ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2008

ADVANCED COMPUTER ARCHITECTURE

SEMESTER - 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) The seek time of a disk is 30 ms. It rotates at the rate of 30 rotations/second. The capacity of each track is 300 words. The access time is approximately

a) 62 ms b) 60 ms

c) 47 ms d) none of these. ☐

ii) The performance of a pipelined processor suffers if.

a) the pipeline stages have different delays

b) consecutive instructions are dependent on each other

c) the pipeline stages share hardware resources

d) all of these. ☐

iii) Consider the high speed 40 ns memory cache with a successful hit ratio of 80%. The regular memory has an access time of 100 ns. What is the effective access time for CPU to access memory ?

a) 52 ns b) 60 ns

c) 70 ns d) 80 ns. ☐

iv) What is a main advantage of classical vector systems (VS) compared with RISC based systems (RS) ?

a) VS have significantly higher memory bandwidth than RS

b) VS have higher clock rate than RS

c) VS are more parallel than RS

d) None of these. ☐

v) Associative memory is a

a) pointer addressable memory

b) very cheap memory

c) content addressable memory

d) slow memory.

vi) The principle of locality justifies the use of

a) Interrupts b) Polling

c) DMA d) Cache memory.

vii) How many address bits are required for a 512 × 4 memory ?

a) 512 b) 4

c) 9 d) $A_0 - A_6$.

viii) A single bus structure is primarily found in

a) Main frames

b) High performance machines

c) Mini and Micro- computers

d) Supercomputers.

ix) What will be the speed up for a four-stage linear pipeline, when the number of instruction $n = 64$?

a) 4.5 b) 7.1

c) 6.5 d) None of these.

x) Dynamic pipeline allows

a) multiples function to evaluate

b) only streamline connection

c) to perform fixed function

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What are the different parameters used in measuring CPU performance ? Briefly discuss each. 5

3. What do you mean by m-way memory interleaving ? In the system with pipeline processing, is the memory interleaving useful ? If yes, explain why. 2 + 3

4. Develop $3^2 \times 4^2$ delta network. 5

5. Compare superscalar, super-pipeline and VLIW techniques. 5

6. Discuss about strip mining and vector stride in vector processors. 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What is Multistage Switching Network ?

   b) Describe the distribution and shared memory model of SIMD architecture.

   c) Draw the block diagram and explain the functionality of processing element.

   2 + 8 + 5

8. a) What is meant by pipeline stall ?

   b) Draw the block diagram of C-access memory function. Why is it necessary and how does it improve the memory access time ?

   c) Implement the data routing logic of SIMD architecture to compute $s(k) = \sum_{i=0}^{k} Ai$ for $k = 0, 1, 2 \ldots N-1$.

   d) A computer has cache access time of 100 nanosecs, a main memory access time of 1000 nanosecs and a hit ratio of 0.9.

      i) Find the average access time of the memory system

      ii) Suppose that in the computer, there is no cache memory, then find the average access time, when the main memory access time is 1000 nanosecs. Compare the two access times. 2 + 4 + 4 + 5

9. a) What is Memory Management Unit (MMU) ?

b) What are the advantages of using cache memory organization ? Define hit ratio. Compare and contrast associative mapping and direct mapping.

c) Draw a 16-input Omega network using 2 × 2 switches as building blocks :

i) Show the switching setting for routing a message from node 1011 to node 0101 and from node 0111 to node 1001 simultaneously. Does blocking exist in this case ?

ii) Determine how many permutations can be implemented in one-pass through this Omega network. What is the percentage of one-pass permutations among all permutations ?

iii) What is the maximum number of passes needed to implement any permutation through the network ? 2 + 7 + 6

10. a) What do you mean by "Data flow Computer" ?

b) With simple diagram, explain Data flow architecture and compare it with control flow architecture.

c) Draw data flow graphs to represent the following computations :

i) X = A + B

ii) Y = X/B

iii) Z = A * X

iv) M = Z – Y

v) N = Z * X

vi) P = M/N.

d) What is vector processor ? Give the block diagram to indicate he architecture of a typical Vector Processor with multiple function pipes. 2 + 6 + 3 + 4

11. Write short notes on any *three* of the following : 3 × 5

a) Omega Network

b) Cross bar Switches

c) Reservation table

d) Multiport Network

e) CM-2 machine.

END