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ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2008

MICROPROCESSOR & MICROCONTROLLERS

SEMESTER – 5

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) The frequency of CLOCK OUT signal of 8085 is

a) 6 MHz b) 3 MHz

c) 6 kHz d) 2 MHz.

ii) Which one of the following is the software interrupt of 8085 A microprocessor ?

a) RST 7·5 b) EI

c) RSTO d) none of these.

iii) If ready pin is grounded, it will introduce ..... status into the bus cycle of 8086/8088 microprocessor.

a) wait b) idle

c) wait & remains idle d) all of these.

iv) What will be the content of PC after execution of the last instruction in the following program ?

$B12B_H$: LXI H, 9100_H
MOV A, M
INR L
ADD M

a) $B130_H$ b) $B12F_H$

c) $B231_H$ d) none of these.

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v) Whenever the POP H instruction is executed

a) data bytes in the HL pair are stored on the stack

b) two data bytes at the top of the stack are transferred to the HL reg. pair

c) two data bytes at the top of the stack are transferred to the PC

d) two data bytes from the HL register that were previously stored on the stack are transferred back to the HL registers.

vi) For 8257 controller ..... is the highest priority channel by default.

a) CH-3 b) CH-0

c) CH-1 d) any channel.

vii) If a DMA request is sent to the microprocessor with a high signal to the HOLD pin, the microprocessor acknowledges the request

a) after completing the present cycle

b) immediately after receiving the signal

c) after completing the program

d) none of these.

viii) In a partial port decoding scheme using 8 bit addressing, two address lines, A1 and A0 are not connected to the decoding NAND gate. Which addresses are made redundant ?

a) $(00)_H, (01)_H, (03)_H, (04)_H$

b) $(00)_H, (02)_H, (13)_H, (14)_H$

c) $(13)_H, (05)_H, (03)_H, (04)_H$

d) $(00)_H, (01)_H, (02)_H, (03)_H$

e) none of these.

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ix) Apart from certain arithmetic operations, RAL/RAR is useful for

a) DMA controlling

b) serial data transfer

c) decimal adjust operations

d) none of these

e) all of these. ☐

x) Mode 5 of 8254 is

a) square wave generator b) rate generator

c) software triggered strobe d) hardware triggered strobe. ☐

xi) The conversion time of a 12 bit successive approximation type A/D converter using an 1 MHz clock is

a) 1 microsecond b) 12 microsecond

c) 4096 microsecond d) 4095 microsecond. ☐

xii) The instruction : EXHG exchanges the contents of

a) Acc & H

b) BC-pair & HL-pair

c) DE-pair & HL-pair

d) HL-pair and a memory location. ☐

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GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Write a program in assembly language for 8085 μP to generate a square wave of 10 kHz with the input clock frequency of 1 MHz of counter 0.

3. In memory mapped I/O, how does microprocessor differentiate between an I/O and Memory ? Can Memory and I/O have the same address ? Compare Memory mapped I/O and Peripheral Mapped I/O. 2 + 1 + 2

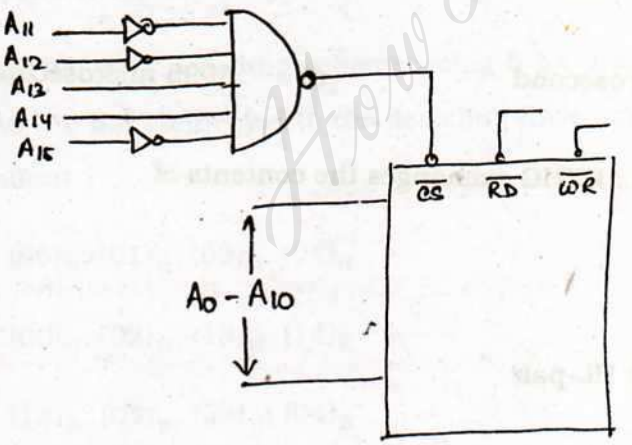
4. a) In the context of 8279 programmable keyboard/display interface, explain the terms "2 key lock out" & "N key roll over".

   b) What do you mean by ICW & OCW ? 3 + 2

5. a) What do you mean by pipelined architecture ? How is it implemented in 8086 ?

   b) Discuss flag register of 8086. 1 + 2 + 2

6. a) Find the memory address range for the following diagram shown below :



   b) Calculate the number of memory chips needed to design 8K-Byte memory if the memory chip size is 1024*1.

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GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) What will be the content of Accumulator and Flag after the execution of following instructions ? 2 + 2

MVI A, 01_H

MVI B, 02_H

ADD B

XRA A

HLT

b) Write an Assembly Language Program to set all the bits of Flag register. 4

c) What are the advantages of indirect addressing mode over direct addressing mode ? 2

d) What do you mean by monitor program ? 2

e) How can microprocessor distinguish between instruction and data ? 3

8. a) Draw the timing diagram of op-code fetch machine cycle. 3

b) What is meant by subroutine ? Briefly discuss the sequence of events that takes place while executing CALL instruction. 4

c) Write an assembly program in 8085 μP to generate some time delay using a register pair. Also calculate the delay for your program, assuming clock period of 320 ns. 5

d) What are RIM and SIM ? Write their functions. 3

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9. a) Draw the block diagram of 8254 timer & briefly discuss its different sections. 5

b) What do you mean by Mode 0, Mode 1, Mode 2 operations of 8255 PPI ? 3

c) Write a BSR control word subroutine to set bits PC_5 & PC_7 & reset them after 10 millisecond. Assume that delay subroutine is available. 2

d) In Mode 1 operation of 8255 PPI, what are the control signals when ports *A* & *B* act as input ports ? Discuss the control signals. 5

10. a) What is the size of data bus and address bus of 8086 μP ? What is the size of addressable memory present in 8086 μP ? 3

b) Explain the operations of BIU and EU present in 8086 μP. 4

c) What are the different types of segment registers present in 8086 μP ? 2

d) What is the difference between MAX Mode operation and MIN Mode operation in 8086 μP ? 4

e) What is the function of $\overline{BHE}$ pin in 8086 μP ? 2

11. a) With respect to 8237 explain the DMA operation. 4

b) What are the priorities of DMA request ? Enumerate them. 3

c) What are the different transfer modes of 8237 ? Explain them in brief. 3

d) How many modes of operation are there in 8253 ? Just name them. 3

e) What is 8279 better known as ? 2

END

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