

Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech(CSE,IT,ECE(O),EIE(O) PWE EEE/SEM-5/EI-502/2009-10

2009

MICROPROCESSOR AND MICROCONTROLLER

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

- i) Whenever the PUSH instruction is executed the stack pointer is
 - a) decremented by 1
 - b) decremented by 2
 - c) incremented by 1
 - d) incremented by 2.

- ii) A single instruction to clear the lower four bits of the accumulator in 8085 microprocessor is
 - a) XRI OFH
 - b) ANI FOH
 - c) ANI OFH
 - d) XRI FOH.

55001

[Turn over

CS/B.Tech(CSE,IT,ECE(O),EIE(O) PWE EEE/SEM-5/EI-502/2009-10

iii) Machine cycles in "CALL" instruction are

- a) 6
- b) 5
- c) 4
- d) 3.

iv) Address lines required for 32 k-byte memory chip are

- a) 13
- b) 14
- c) 15
- d) 16.

v) For 8255 PPI the bi-directional mode of operation is supported in

- a) Mode 1
- b) Mode 0
- c) Mode 2
- d) Either (a) & (c).

vi) The CWR address of 8255 connected to 8085 is FBh. What will be the address for Port A ?

- a) F8h
- b) FA h
- c) FC h
- d) F9 h.

vii) The Segment and Offset address of the instruction to be executed by 8086 microprocessor are pointed by

- a) CS AND SI
- b) DS and IP
- c) CS and SP
- d) CS and IP.

viii) Mode 2 of 8253 is

- a) Square wave generator
- b) Rate generator
- c) Software trigger stroke
- d) Hardware trigger strobe.

ix) PSW is a register.

- a) 8 bit
- b) 16 bit
- c) 20 bit
- d) 32 bit.

x) If READY pin is grounded, it will introduce states into the bus cycle of 8086 microprocessor.

- a) wait
- b) idle
- c) wait and remain idle
- d) all of these.

xi) The call location for TRAP interrupt is

- a) 0000h
- b) 0020h
- c) 0024h
- d) 0034h.

xii) In order to enable TRAP interrupt, which of the following instructions is are needed ?

- a) EI only
- b) SIM only
- c) EI and SIM
- d) none of these.

xiii) In 8085 microprocessor, the addressable memory is

- a) 64 KB
- b) 1 MB
- c) 4 KB
- d) 16 KB.

- xiv) What is the length of SP (stack pointer) of 8085 μ P ?
- a) 6 bits
 - b) 8 bits
 - c) 12 bits
 - d) 16 bits.
- xv) What will be the content of the accumulator and status of CY flag after RLC operation, if the content of the accumulator is BC H and CY is 0 ?
- a) 79 H, 1
 - b) 78 H, 1
 - c) 5E H, 0
 - d) 5D H, 0.

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) Differentiate between peripheral mapped I/O and memory mapped I/O.
- b) What are the functions of ALE, HOLD and READY ?
3. The following sequences of instructions are executed by 8085 μ P :

- C000 LXI SP, D050
- C003 POP H
- C004 XRA A
- C005 MOV A, H
- C006 ADD L
- C007 MOV H, A
- C008 PUSH H
- C009 PUSH PSW
- C00A HLT

D050	05
D051	40
D052	52
D053	03
D054	XX

What are the contents of Stack Pointer (SP), Program Counter (PC), Accumulator and HL pair ?

4. Discuss the functions of following instruction of 8085 : 5×1

RAR, LHL D C020H, DAD, CALL D050H, DCX B

5. What are the advantages of having segmentation ? How does 8086 μ P support sementation ? $3 + 2$

6. What is subroutine ? What is the difference between CALL & JMP instructions ? $2 + 3$

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) How many ports are there in 8255 and what are they ?
- b) Discuss the different bits of the control word of 8255.
- c) Write down the MODE-0 control word for the following :
- i) Port A = Input
 - ii) Port B not used
 - iii) Port C upper = Input, Port C lower = output.
- d) Discuss BSR operation of 8255. $2 + 5 + 3 + 5$

CS/B.Tech(CSE,IT,ECE(O),EIE(O) PWE EEE/SEM-5/EI-502/2009-10

8. a) Explain how 20-bit physical address is generated in 8086 microprocessor.

b) What is the purpose of queue ? How many words does the queue store in the 8086 microprocessor ?

c) How does 8086 support pipelining ? Explain.

d) What are the advantages of having memory segmentation ? $3 + (1 + 3 + 5 + 3)$

9. a) Describe the priority scheme & EOI scheme of 8259.

b) Write down the format of ICW1 & ICW2 of 8259.

c) With respect to 8237 explain the DMA operation.

$5 + 5 + 5$

10. a) Write a program to find out the largest number, starting from D000 H of 10 numbers and store result in D050 H.

b) Write a program to find out square of a data using LookUp table. $7\frac{1}{2} + 7\frac{1}{2}$

55001

6

CS/B.Tech(CSE,IT,ECE(O),EIE(O) PWE EEE/SEM-5/EI-502/2009-10

11. a) What are the vectored and non-vectored interrupts ?
- b) Explain the instruction RIM and SIM. Write the program for enable the RST-7.5, RST-6.5 and disable RST-5.5.
- c) Discuss how 8253 is used to generate square wave.
- d) What are the major components of 8259A interrupt controller ? Explain their functions.
- e) Write the BSR control word for setting PC₄ in 8255A.

2 + 5 + 3 + 3 + 2

=====