COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE (SEMESTER - 2)

CS/BCA/SEM-2/BCA-201/08

1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

CS/BCA/SEM-2/BCA-201/08

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2008

COMPUTER ARCHITECTURE AND SYSTEM SOFTWARE (SEMESTER - 2)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. **This Booklet is a Question-cum-Answer Booklet.** The Booklet consists of **32 pages**. **First page** of the Booklet shows Instructions to the Candidates. The **questions** of this concerned subject commence from **Page No. 3**.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. Fill in your Roll No. in the box provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. Use of Mobile Phone, Calculator or Log table is totally prohibited in the examination hall.
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, which will lead to disqualification.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B			Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

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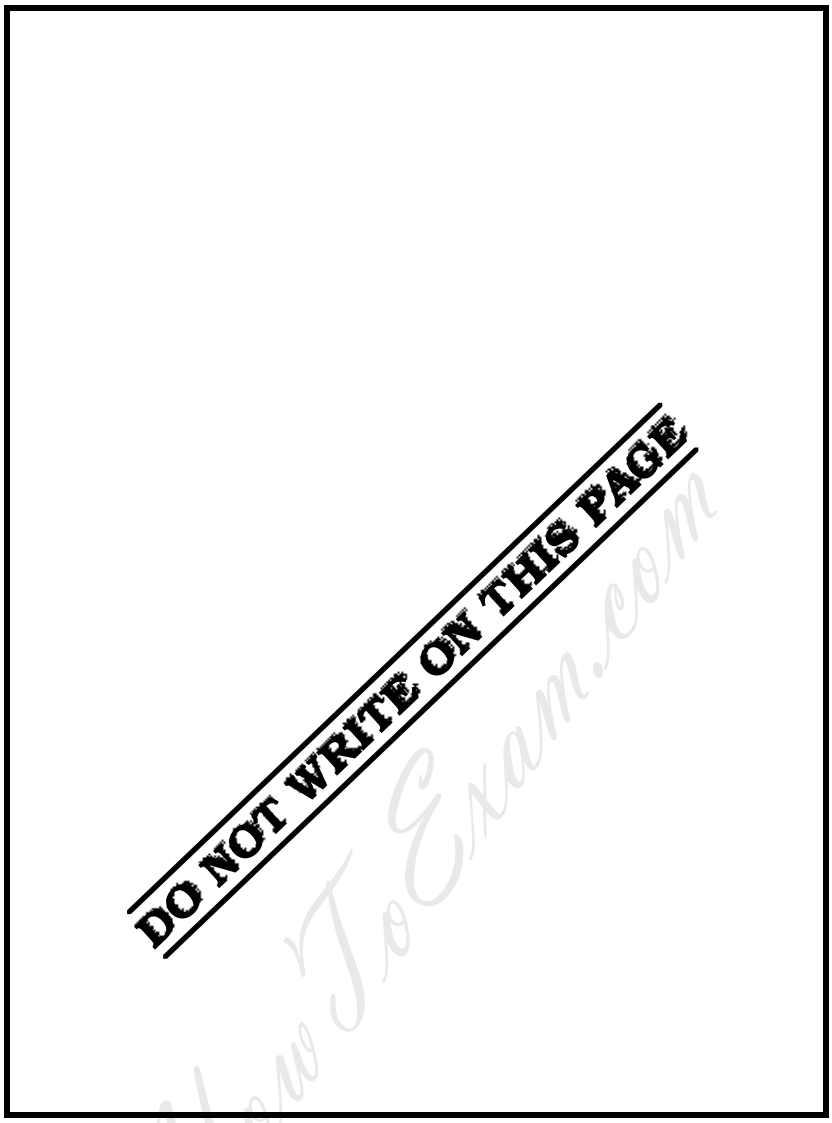
Head-Examiner/Co-Ordinator/Scrutineer

II-222444 (1)



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GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) The instruction LOAD A is a

a) zero-address instruction b) one-address instruction

c) two-address instruction d) three-address instruction.

ii) The purpose of cache memory in a computer is to

a) ensure fast booting b) reduce load on CPU registers

c) replace static memory d) speed up memory access.

iii) Object code is

a) input to assembler b) output of assembler

c) intermediate code d) none of these.

iv) Which of the following is not an advantage of Dynamic RAMs ?

a) High density

b) Low cost

c) High speed

d) No need of memory refresh.

v) DMA module can communicate with CPU through

a) interrupt b) cycle stealing

c) branch instruction d) none of these. ☐

vi) The number of fetch operation(s) to execute instruction in immediate mode is

a) 0 b) 1

c) 2 d) none of these. ☐

vii) A CPU has 16-bit program counter (PC). This means CPU can address ..... memory locations

a) 16K b) 32K

c) 64K d) 256K. ☐

viii) The major objective in choosing page replacement policy is to

a) minimize hit ratio b) reduce size of page

c) maximize hit ratio d) none of these. ☐

ix) The sum of $(24D)_{16}$ and $(9AA)_{16}$ is

a) $(BE7)_{16}$ b) $(BF6)_{16}$

c) $(AF7)_{16}$ d) $(BF7)_{16}$. ☐

x) In a stack computer, there is support for

a) PUSH and POP instruction only

b) zero address instruction only

c) zero address instruction, PUSH and POP

d) none of these. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Convert the hexadecimal number FCO6 into decimal, binary and octal.

3. In floating-point number representation system, if 24 bits are reserved for mantissa and 8 bits are reserved for signed exponent, determine the values of maximum & minimum positive & negative numbers in this scheme.

4. Why are sub-routines written & used ? What is a stack ? What are the operations that can be performed on stack ? What is a 'macro' ? What is the basic difference between a 'macro' and a 'sub-routine' ?

5. Write down the Register Transfer Language for execution of

   LDAX B

   STAX D

6. Comment on Direct Mapping Function of 2048 word Cache Memory onto 65,536 word Main memory.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) What is virtual memory ? What could be the maximum size of virtual memory ? Justify. 3

   b) Briefly describe an instruction execution cycle with proper timing diagram. 3

   c) Explain the Booth's algorithm. Illustrate with example. 3

   d) Briefly discuss different types of ROM. 3

   e) Differentiate between static RAM and dynamic RAM. 3

8. a) What are the differences between RISC and CISC processors ? 4

   b) Explain the concepts of sequential processing, pipelining and parallel processing with examples. 6

c) What are the elements of a machine instruction ? 3

d) What is meant by memory access time ? 2

9. a) What is meant by random access and sequential access of memory devices ? Explain. 4

b) What is hit ratio in a two-level memory system ? 3

c) Provide the architecture of CPU. 4

d) Given a task that can be divided into m subtasks, each requiring one unit of time, how much time is required for an m-stage pipeline to process n tasks ? 4

10. a) Discuss the efficiency and throughput of a k-stage pipeline system processing n tasks. 5

b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with clock cycles of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved ? 5

c) Explain paging in Memory with suitable examples. 5

11. a) It is desired to have 5kB of memory in a computer. 4kB should be ROM and 1kB should be RAM. You have to design the chip-select signals of Memory-chips in such a way that first 4k addresses should select ROM and next higher 1k addresses should select RAM. You have been given a number of ROM chips (namely 2716 which is 2k × 8) and RAM chips (namely 2142 which is 1k × 4).

b) Describe Set Associative Mapping Function of 2048 word Cache Memory on 65,536 word Main Memory.

c) Describe in detail how physical address is generated from Virtual address using Virtual memory technique.

d) What is parallel processing ? 5 + 5 + 3 + 2

END