FACULTY OF ENGINEERING

B.E. 4/4 (ECE) (I-Semester) Supplementary Examination, April, 2006

DIGITAL DESIGN WITH HDL

Time : Three Hours] [Maximum Marks : 75

*Answer **All** questions of Part A.*

*Answer **FIVE** questions from Part B.*

PART—A

(Marks : 25)

1. What are the three basic description styles supported by verilog HDL ?
2. What are the two main data types in verilog HDL ?
3. Name two swith-level modeling primitive gates.
4. What is the purpose of the 'time scale' compiler directive ?
5. State two ways by which you can override a parameter value at compile time.
6. Declare a parameter GATE-DELAY with a value of 5.
7. How is a combinational UDP different from a sequential UDP ?
8. When there are two or more assignments to the same target, how is the effective value for the target determined ?
9. When is a label required for a block ?
10. How does the case x statement differ from case statement ?

PART—B

(Marks : 5×10=50)

11. (a) What are the bit patterns for the following :

    7'044, 'B x 0, 5'b x 110, 'hA0, 10'dz, 'hzf.

    (b) Explain the text substitution directive using an example.

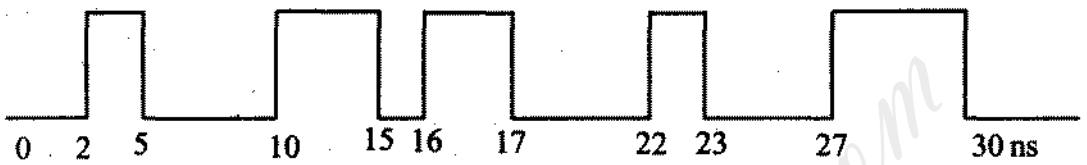
12. (a) What is the difference between a sequential block and a parallel block ? Explain using an example. Can a sequential block appear within a parallel block ?

    (b) What is the difference between an intra statement delay and an inter statement delay ? Explain using an example.

13. (a) Write a function that converts a four-character string that contains only decimal digits to an integer value. For example if My Buffer contains the string "4298", convert it to an integer MyInt that has the value 4298.

(b) Write a task that dumps the contents of a memory starting from a specified begin and end locations.

14. (a) Write a VHDL model that generates the waveform shown in figure below :



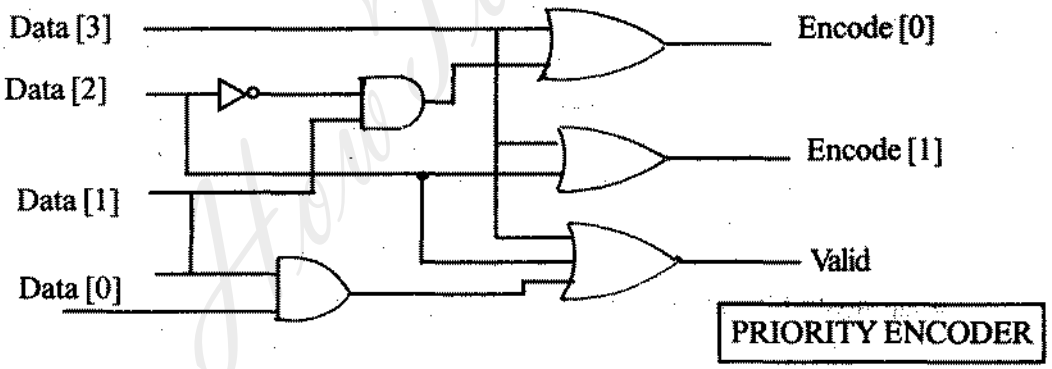
(b) Describe an ALU that performs on the relational operations (<, >=, >, >=) on two 4-bit operands. Write a test bench that reads the test patterns and the expected result from a textile.

15. (a) Describe a D-type flip-flop using behavioural construct, then using this module, write a model for a g bit register.

(b) Show how a disable statement can be used to emulate the behaviour of the "continue" and "break" statements of the C programming language.

16. (a) Describe the behaviour of a JK flip-flop using an always statement.

(b) Write a user-defined primitive (UDP) description for the priority encoder circuit shown in figure below :



17. (a) Write an expression that performs the arithmetic shift of a 8-bit signed number contained in Q parity.

(b) Given a 32-bit bus, Address-Bus, write an expression that computer the reduction n and of bits 11 through 20.