Code No.: 10294

FACULTY OF ENGINEERING

B.E. III/IV Year (ECE) I Semester (Supplementary) Examination, May 2006

DIGITAL INTEGRATED CIRCUITS AND APPLICATIONS

Time : 3 *Hours*] [*Max. Marks* : 75

Answer **all** *questions of* Part A.
Answer **five** *questions from* Part B.

Part A – (Marks : 25)

1. Show the circuit diagrams of AND, OR, NOT in DTL family. 3
2. Write three advantages of CMOS logic. 3
3. Write the description of the following ICs : 3
   (a) 74 ALS00 (b) 74 HS00 (c) 74 LS32
4. Distinguish between an encoder and decoder. 2
5. What are the advantages of synchronous counters? 3
6. Show the diagram of a 3-bit binary up counter. 2
7. Distinguish between ROM, static RAM and dynamic RAM. 3
8. Define memory word and memory cell. 2
9. Write the advantages of PLDs. 2
10. What is the difference between FPGAs and gate arrays? 2

Part B – (Marks : 5 × 10 = 50)

11. (a) Explain IC interfacing techniques for CMOS and TTL families. 5
    (b) Draw the circuit diagram of a 2-input ECL NOR/OR gate and explain the operation with the truth tables. 5

12. (a) Design a gray to BCD converter using (i) Dual 4:1 multiplexor IC and same gates. 5
    (b) Design a 4-bit magnitude comparator and show the logic diagram. 5

13. (a) What is the race around problem in J-K flip flop? Explain how it is eliminated in J-K MS flip flop. Show the truth tables. 5
    (b) Explain the operation of a 4-bit universal shift register with circuit diagram. How do you realize a Johnson counter using shift register? 5

14. (a) Realize a 32K byte RAM system using 16K × 4 memory chips. Give the address map. 5

(b) Draw the structure of a DRAM cell and explain its function. Also explain DRAM refreshing and address multiplexing. 5

15. (a) Compare PAL and PLA with the help of block schematics and explain the respectives advantages. 5

(b) Discuss full custom and semi custom ASKs and their architectures. 5

16. (a) Design a Mod-6 asynchronous counter using T-FFS with clear inputs. Explain its function using timing diagram. 5

(b) Draw the circuit diagram of an R-S latch and explain. Discuss how a debounce circuit eliminates the problems of this circuit. 5

17. (a) Design and explain with waveforms the operation of a divided by-12 ripple counter. What are the advantages of ripple counters? 5

(b) Explain parallel, serial and fast-serial binary adders with circuit diagrams. 5