Code No.10544/N

FACULTY OF ENGINEERING

B.E.4/4 (ECE) II-Semester (New) Main Examination,April 2006

Subject: Design of Fault Tolerant Systems

(Elective-II)

Time: 3 Hours. Max.Marks: 75

Note: Answer all questions of Part A and any five questions from Part B.

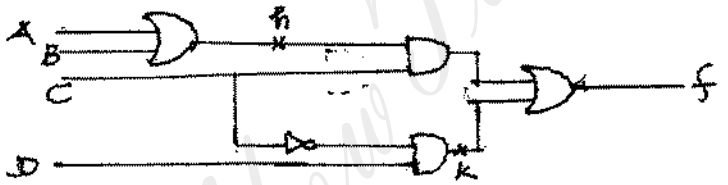
PART-A (25 marks)

1. Define the following: 3
   a) Reliability b) Availability c) Maintainability
2. What is MTBF. 2
3. Differentiate between transient and intermittent faults. 3
4. What is Fail-Soft operation. 2
5. Differentiate between observability and controllability. 3
6. What is meant by Fail Safe design. 2
7. Mention the advantages of LSSD technique. 3
8. What is pluribus and where do you use it. 2
9. What is self-checking PLA. Give its structure. 3
10. Define the terms BIOCO/BILBO. 2

PART-B (5x10=50 marks)

11. a) What are temporary faults and what are the techniques that are used to present them. 3

    b) For the circuit below find the tests to detect S-a-0 and S-a-1 faults h and k by using Boolean difference method. 7



12. What is fault-tolerance. Explain in detail the method of fault tolerance by a) Static redundancy b) self-purging redundancy c) Hybrid redundancy. 10
13. a) Design a check bit generator circuit for totally self checking checker for Berger code for the case information bits I = 7, check bits = 3. 7

    b) Write short notes on self-checking checker for Lowcost residue code. 3
14. Explain in detail, the features, rules and advantages of LSSD testable circuits. 10
15. Explain in detail 'The Reed-Muller expansion technique' and '3 level OR-AND-OR design' for realization of testable combinational logic circuits. 10
16. Explain about Sift-out Modular redundancy (SMR) along with its comparator, detector and collector circuits for 3-channel SMR. 10
17. Write short notes on:
    1) Stuck at faults
    2) TWO rail checker
    3) Random Access Scan technique.