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BT-4/M09 9329

Digital Electronics

Paper : EE-204-E

Time : Three Hours] [Maximum Marks : 100

Note :- No. of questions to be attempted : **FIVE**, by selecting at least one from each unit.

UNIT-I

1. (a) Decode the following ASCII code : 1001010 1100001 1101110 1100101 0100000 1000100 1101111 1100101.

   (b) The following is a string of ASCII characters whose bit patterns have been converted into hexadecimal for compactnessT: 4A EF 68 6F 20 C4 EF E5. Of the 8 bits in each pair of digits, the leftmost is a parity bit. The remaining bits are the ASCII code.

   (i) Convert to bit form and decode the ASCII

   (ii) Determine the parity used : odd or even.

2. Given the Boolean function :

   $$F = xy\,z + x\,y\,z + w\,xy + wx\,y + wxy$$

   Obtain the truth table of the function.

   (i) Draw the logic diagram using the original Boolean expression.

   (ii) Simplify the function to a minimum number of literals using Boolean algebra. Obtain the truth table of the function from the simplified expression and show that it is the same as the one obtained in part (i).

   (iii) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part (ii).

UNIT-II

3. (a) Design a combinational circuit that generates the 9's complement of a BCD digit.

   (b) Design a BCD-to-decimal decoder using the unused combinations of the BCD code as don't care conditions.

4. Design a sequential circuit with two JK flip-flops A and B and two inputs E and x. If E = 0, the circuit remains in the same state regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

UNIT–III

5. (a) A flip-flops has a 5 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops ? What is the maximum frequency the counter can operate reliably ?

(b) Design a counter with T flip-flops that goes through the following binary repeated sequence : 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.

6. (a) (i) Explain the differences between asynchronous and synchronous sequential circuits.

(ii) Define fundamental-mode operation.

(iii) Explain the difference between stable and unstable states.

(iv) What is the difference between an internal state and a total state ?

(b) An asynchronous sequential circuit is described by the excitation and output functions :

$$Y = x_1x_2 + (x_1 + x_2)\, y$$

$$z = y$$

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map.

(iii) Obtain a two-state flow table.

(iv) Describe in words the behavior of the circuit.

UNIT–IV

7. (a) Using the actual output transistors of two open-collecter TTL gates, show (by means of a truth table) that when connected together to an external resistor and V_{cc}, the wired connection produces an AND function.

   (b) Prove that two open-collector TTL inverters, when connected together, produce the NOR function.

8. (a) Determine the high-level output voltage of the RTL gate for a fan-out of 5.

   (b) Determine the minimum input voltage required to drive an RTL transistor to saturation when $h_{FE} = 20$.

   (c) From the results in (a) and (b), determine the noise margin of the RTL gate when the input is high and the fan-out is 5.