Roll No. ..... Total No. of Pages : 3

BT-4/J07 8764

Digital Electronics

Paper-ECE-204 E

Time : Three Hours] [Maximum Marks : 100

Note :- Attempt **FIVE** questions in all, selecting at least **ONE** question from each part. **Each** question carries **equal** marks.

PART-I

1. Perform the indicated operation :-
   (i) Determine the decimal value of $(0.325)_8$.
   (ii) Discuss the self complementing property of excess-3 code.
   (iii) Add the following BCD numbers :-
   01100111 + 01010011
   (iv) Convert $(2469)_{10}$ to BCD.
   (v) Subtract $94_{16} - 5C_{16}$.
   (vi) Convert $F80B_{16}$ to Binary.
   (vii) Divide 01100100 by 00011001 using sign magnitude arithmetic.
   (viii) Subtract the following binary numbers (Signed Number) :-
   00001100 – 11110111.
   (ix) Find 2's complement of 10111000.
   (x) Multiply the binary numbers : 101 × 111. 10×2=20

2. (a) Using Q-M algorithm find a minimal cover for the following function :-
   $F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 10) + d(3, 11, 15)$. 15

(b) Draw the circuit and discuss their characteristic tables for the following gates :–

(i) OR gate using NAND gates only.

(ii) EX-OR and EX-NOR gates using NOR gates only. 5

PART–II

3. (a) A combinational circuit is defined by the fallowing three functions :–

$$F_1 = \overline{X} + Y, \quad F_2 = XY + \overline{X}\,\overline{Y}$$

$$F_3 = \overline{X}\,\overline{Y} + XY\overline{Z}$$

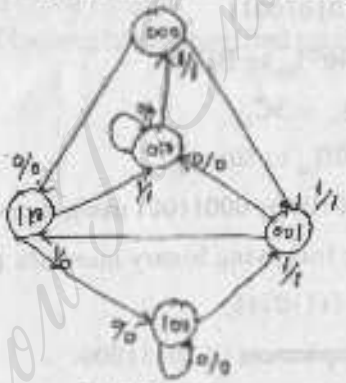
Design the circuit with a decoder and external gates. 10

(b) Draw a logic diagram of 2-line to 4-line decoder / demultiplexer using NOR gates only. 5

(c) Design a 3-Bit Binary to Gray Code Converter. 5

4. (a) Draw a 4-Bit parallel-in serial-out shift register. Draw the timing diagram for outputs. 10

(b) For the state diagram shown below, design the circuit using 'D' FFs.



10

PART–III

5. (a) What is basic difference in saturated and non saturated logic families ? Describe the operation of a basic ECL and prove that the transistors in ECL are never driven to saturation region. 10

(b) What are the limitations of DTL over TTL ? 5

(c) Modify 'DTL' circuit to use in high noise environment. 5

(a) What is Interfacing ? Discuss the interfacing between CMOS and TTL. 10

(b) Discuss the advantages and disadvantages of CMOS over TTL. 5

(c) Explain the operation of a CMOS NOR gate. 5

PART–IV

(a) Write a short note on each of the following :–

(i) Weighted Resistor DAC

(ii) Dual Slope ADC. 10

(b) Explain the specifications for ADC and DAC which must be satisfied. 10

(a) Design a BCD to Excess -3 Code converter using a

(i) PROM (ii) PLA (iii) PAL. 15

(b) Discuss the architecture for a PLD. Give some suitable examples. 5