MODEL QUESTION

B.Tech. Degree Examination Nov./Dec. 2010

FIFTH SEMESTER COMPUTER SCINCE & ENGINEERING

08.505 MICROPROCESSORS AND INTERFACING

Time:3 Hours

Maximum Marks 100

PART A

(Answer **ALL** questions, each carries 4 marks) [10 x 4 = 40]

1. Any information in the memory of a computer is stored as 1s and 0s. How does the processor know an item stored in a memory location is a data or an instruction?
2. Draw the timing diagram for op-code fetch.
3. Illustrate how the low-order address bus of 8085 is de-multiplexed
4. Explain the principle of working of successive – approximation A/D converter.
5. Compare and contrast 8086 microprocessor with 8088.
6. Explain the function of the following signals of 8086 :
   (a) $\overline{TEST}$ (b) $\overline{LOCK}$ (c) $MN/\overline{MX}$ (d) READY
7. Write an assembly language program to find the largest number in a given unordered array of 8-bit numbers.
8. Write a program segment to generate a pulse every 50 micro second from counter 0 of 8254. The address of counter 0 is 80H and the clock speed of 8086 is 2MHz.
9. List major components of 8251 USART and mention their functions.
10. An 8255A has a system base address of FFF9H. Write the initialization commands required to program all ports 8255A as output ports in mode 0.

PART B

(Answer **one FULL** question from each module) [3 x 20 = 60]

Module 1

11 (a) With a diagram, explain the functional units of 8085 microprocessor (12 Marks)

(b) It is required to interface one chip of 16K x 8 ROM and one chip of 32K x 8 RAM with 8085. ROM address starts at 0000H. Show the implementation of this memory system.

OR (8 Marks)

12(a) Draw and explain the schematic of a micro computer by illustrating processor, memory modules, address bus, data bus and control signals (10 Marks)

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(b) Explain with a diagram how a 12-bit DAC(Digital to Analog Converter) can be interfaced with 8085 microprocessor.

If the DAC is calibrated over the range 0 to 10V calculate the outputs if the Input is 01H and 82H. (10 Marks)

Module 2

13(a) Explain the physical memory organization in an 8086 system. What is the maximum memory addressing and I/O addressing capability of 8086 ? (10 Marks)

(b)Write an 8086 based assembly language program to sort a set of 100 sixteen bit numbers in non- decreasing order (10 Marks)

OR

14(a) Explain the functional units of 8259 Interrupt controller (12 Marks)

(b)Write 8086 based initialization instructions and commands for 8259 to meet the following specifications: (i) Single (ii) Level triggered (iii) Call address interval 4 (iv) Interrupt type 40 corresponds to IR0 input (v) Normal EOI (vi)Non buffered mode (vii)Not specially fully nested mode (viii) IR1 and IR3 unmasked. The base address of 8259 is FF10H. (8 Marks)

Module 3

15(a) Discuss the various modes operation of 8255 Programmable Peripheral Interfacing.

An 8255A has a system base address of FFF10H. What are the system addresses for the three ports and the control register for this 8255A. Show the BSR mode control words needed to initialize an 8255 (i) to set PC3(ii) to reset PC3 (12 Marks)

(b) Describe the series of actions that a DMA controller will perform after it receives a request From a peripheral device to transfer data to memory. (8 Marks)

OR

16(a) Explain the idea of multiplexing a seven digit 7-segment display. (10 Marks)

(b) Explain the various functional units of 8279 used to control the key board and display of a system (10 Marks)