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Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, July 2008

(2003 Scheme)

03.606 : Elective – II : DESIGNING WITH VHDL (TA)

Time: 3 Hours Max. Marks: 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Define entity declaration in VHDL. Write the entity declaration for the half-adder.
2. Give two examples each for basic identifiers and extended identifiers.
3. Write the data flow model for a 1 bit full adder.
4. Explain, with the help of an example the use of NEXT statement.
5. Write a VHDL function that performs byte reversal.
6. Define a procedure body that implements an ALU with the following operations : ADD, SUB, MUL, DIV.
7. What are the components of a design file in VHDL ?
8. Define a test bench. Give the general format of a test bench.
9. Write the VHDL code to initialize 256 locations of 8 bit memory to OOH.
10. What are the major timing specifications of CPLD ? **(10×4=40 Marks)**

P.T.O.

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. What are the 4 classes of data objects ? Give examples for each of them and explain.

12. Describe the predefined operators in VHDL, with examples.

13. Implement the structural and behavioural models of a 4x1 Mux using VHDL.

Module – II

14. Write a procedure for converting 3 bits of binary into octal in VHDL.

15. Write a procedure for converting 4 bit binary to gray code, in VHDL.

16. Implement a primitive ALU that can perform the following operations :

    ADD, SUB, MUL, DIV, LT, LE, EQ.

Module – III

17. Draw the functional block diagram of any commercial FPGA and explain its features.

18. Implement a barrel shifter in VHDL. It should rotate the input data by the specified number of bits. Give 2 different architectural bodies for implementing the barrel shifter in VHDL.

19. Implement a generic model of a divide-by-2 * N clock generator in VHDL.