(Please write your Exam Roll No.) Exam Roll No. ....169.....

END TERM EXAMINATION

FOURTH SEMESTER [B.TECH.] – MAY-JUNE 2009

Paper Code: ETEC-206 Subject: Digital Circuits & System-I
Paper ID: 28206 (Batch: 2004-2007)
Time : 3 Hours Maximum Marks :75

Note: Attempt any five questions.

Q.1 (a) Which of the following are incorrect representation and why? (5)
(i) 1010011_{bcd} (ii) 0208_{octal} (iii) 10102011_{binary}
(iv) $GCOA_{hexadecimal}$ (v) $120A_{decimal}$
(b) Divide a number 0111 1011 111 1001 by divisor 0111 1111 1110 0011. (5)
(c) Show by an example that we can subtract both positive and negative numbers by two's complement arithmetic. (5)

Q.2 (a) Simplify A.C + A.(C+B) + C.(C+B) using Boolean rules and draw the simplest possible logic circuit. (4)
(b) Convert POS $(A+B+\overline{C.D})$ expression into standard four variables POS format four variables. (4)
(c) Simplify after first converting $(A.\overline{B}.C)+(\overline{A}.C.D)$ to standard POS form and then using K map to make a circuit with NOR gates only. (7)

Q.3 (a) Design and implement the function F = Π M (1, 7, 9, 15) using 4:1 MUX. (8)
(b) Give logic design and implement the Boolean functions $F_1 = \Sigma$ m (3, 7, 9, 10) and $F_2 = \Sigma$ m(2, 7, 12, 15) using decoder. (7)

Q.4 (a) Explain why gated SR latch is called a transparent latch? Show the timing diagram for gated SR later with clock input (active level 1). (7)
(b) Consider a JK' flip flop i.e. a JK flip flop with an inverter between external input K' and internal input K. (i) Obtain the flip flop characteristics table (ii) obtain the characteristic equation (iii) show that tying the two external inputs together forms a D flip flop. (8)

Q.5 (a) Explain the working of Modulo-10 (decode) counter and implement the logic circuit using JK ff. (8)
(b) Design a 4-bit buffer register with parallel output after storing. (7)

Q.6 (a) An astable multivibrator uses timer 555. It is required that duty cycle is 0.58 and frequency is 10 KHz. If capacitor used is of .001 μF then find the value of resistances to obtain desired duty cycle. Can we obtain duty cycle of 0.5? (7)
(b) If digital output of a 12-bit ADC is 1000 0111 1111 then find the resolution and the input at that instance when $V_{ref}/2 = 0.75V$. (4)
(c) Give circuit diagram and explain working of successive approximation ADC. (4)

Q.7 (a) Explain following terms w.r.t. logic families (i) speed (ii) propagation delay (iii) operating frequency (iv) power dissipated per gate (v) fan out (vi) fan in (vii) noise immunity (viii) V_{OH}, V_{IH}, V_{OL}, V_{IL}. (8)
(b) Compare and contrast MOS and Bipolar logic families. Also give applications. (7)

Q.8 (a) A dynamic RAM needs refresh every few milli seconds and a static RAM need not. Why? (7)
(b) Differentiate between PAL & PLA. What is the advantage of tristate outputs and registered outputs provision in PAL? (8)

Q.9 Write short notes (**any three**) :- (15)

(a) Content addressable memory
(b) Binary-weighted DAC
(c) Nyquist sampling theorem
(d) Drivers for display devices
(e) Don't care conditions

****