B.Tech. Degree VII Semester Examination, November 2006

EC 703 VLSI DESIGN

(2002 Admissions onwards)

Time: 3 Hours Maximum Marks: 100

I	a)	Draw and explain the process of n-well CMOS fabrication.	(8)
	b)	Discuss the flow diagram of n-well technology.	(6)
	c)	Compare between monolithic and hybrid IC's and also mention about its application areas?	(6)
		OR	
II	a)	Explain why GaAs is preferred than Si in microwave monolithic IC's.	(5)
	b)	Compare the material properties of GaAs and Si.	(5)
	c)	Discuss about the high current and high energy ion implantation equipment and explain how it varies from a typical ion implanter with relevant diagram.	(10)
III	a)	Derive an expression for drain current for long channel MOSFET and explain the various modes of operation under different voltages.	(10)
	b)	Discuss about various second order effects in MOSFETS.	(10)
		OR	
IV	a)	Derive an expression for pull up to pull down ratio for an NMOS inverter driven by another NMOS inverter.	(10)
	b)	A PMOS structure has a substrate doping of $N_d=10^{16}cm^{-3}$ and a gate doping of $N_d=10^{20}cm^{-3}$. The oxide charge density is $Q_{ox}=4 \times 10^{10}$ $q=6.4nC/cm^2$ and thickness is $t_{ox}=1000$ angstroms. • Calculate the threshold voltage with zero substrate bias • Calculate the body coefficient γ	(10)
V		Discuss the need of design rules? What is the difference between λ rules and micron rules. Draw the circuit diagram; stick diagram and layout of a two input CMOS NAND gate?	(20)
		OR	
VI	a)	Discuss the need of super buffers and explain the working of inverting and non-inverting super buffers.	(10)
	b)	Explain the concept of sheet resistance and MOS device capacitance with relevant Equations.	(10)
VII	a)	Discuss the various implementation strategies of digital IC's.	(10)
	b)	Explain the working of clocked CMOS (C^2MOS) logic with diagram.	(10)
		OR	
VIII	a)	Explain the working of a two input XNOR gage using pass transistors.	(5)
	b)	Implement the function Z=(A.B)+(C.D) using CMOS logic and draw its stick diagram.	(15)
IX	a)	What is clock skew and discuss the effect of positive and negative clock skew on clock period with relevant diagrams and equations?	(10)
	b)	Explain the concept and implementtion of synchronizers.	(10)
		OR	
X		Write ***short notes*** on: (i) Synchronous versus asynchronous (ii) Self timed circuit design (iii) Clock distribution techniques	(20)

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