BTS (C) – IV– 09 – 013 – E

B. Tech Degree IV Semester Examination, April 2009

EE 402 LOGIC DESIGN

(2006 Scheme)

Time : 3 Hours Maximum Marks : 100

PART - A

(8 x 5 = 40)

I. (a) (i) Convert $110101 \cdot 101010_2$ to octal.

(ii) Convert $4BAC_{16}$ to binary.

(iii) Convert the Gray Code 1101 to binary.

(b) Prove that $AB + \bar{A}C + BC = AB + \bar{A}C$.

(c) Compare serial and parallel adders.

(d) Design and implement a full subtractor using X-OR gates.

(e) Differentiate between PLA and PAL.

(f) Design a D – flip flop using J – K flip flop.

(g) Explain the terms fan out, speed of operation, power dissipation, figure of merit and noise margin with respect to digital Ic's.

(h) Explain tri-state logic.

PART - B

(4 x 15 = 60)

II. (a) Simplify the expression using *K* map and realize using *NOR* gates

$$\sum m(1,5,6,12,13,14) + d(2,4)$$ (8)

(b) Implement a binary to octal decoder having active high o/p. (7)

OR

III. (a) Simplify the expression using Quine Mc Chusky method

$$\sum m(0,1,6,7,8,9,13,14,15)$$ (10)

(b) Use a multiplexer to implement the logic function $F = A \oplus B \oplus C$ (5)

IV. (a) Draw the logic diagram of a 4 stage look – ahead carry adder. (8)

(b) Explain how a look ahead carry adder speeds up the process of eliminating ripple carry delay. (7)

OR

V. (a) Draw the ckt of an astable multivibrator using discrete gates. Explain its working with timing diagram. (7)

(b) Design and implement a full adder using NAND gates. (8)

VI. (a) Convert a S – R flip flop to J – K flip flop and draw the logic diagram. (8)

(b) Design and implement a mod – 6 asynchronous counter using TFFS. (7)

OR

VII. (a) Design a type T counter that goes through the states $(0,3,5,6,0)$. Is the counter self starting? (8)

(b) Draw the architecture of programmable logic device and explain. (7)

VIII. (a) Explain with circuit diagram the operation of typical 3 input TTL NAND gates. (8)

(b) Draw a 2 – input CMOS NAND gate. (7)

OR

IX. (a) Draw the circuit of an ECL nor gate and explain its operation. (8)

(b) Explain two methods of interfacing TTL to CMOS logic. (7)

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