B.Tech Degree IV Semester (Supplementary) Examination January 2011

EI/EE 404 COMPUTER ARCHITECTURE AND ORGANISATION

(2002 Scheme)

Time : 3 Hours Maximum Marks : 100

I.	(a)	Explain various addressing modes available in a general computer with example.	(15)
	(b)	What is emulating?	(5)
		OR	
II.	(a)	Explain Booth's algorithm with an example.	(10)
	(b)	Explain micro programmed control.	(10)
III.	(a)	Explain the principle of operating of cache memories. Discuss the different mapping techniques associated with cache memories.	(15)
	(b)	Define the following :	
		(i) Write through protocol	(2 ½)
		(ii) Write back protocol	(2 ½)
		OR	
IV.	(a)	Explain virtual memory address translation.	(15)
	(b)	Explain the concept of memory interleaving.	(5)
V.	(a)	Explain Direct Memory Access.	(10)
	(b)	Give the sequence of events involved in handling an interrupt request from a device.	(10)
		OR	
VI.	(a)	Explain about vectored interrupts.	(10)
	(b)	Explain :	
		(i) Daisy chaining	(5)
		(ii) Cycle stealing	(5)
VII.		Explain the architecture of 8085 with its functional block diagram.	(20)
		OR	
VIII.	(a)	Explain the various hardware interrupts of 8085.	(10)
	(b)	Explain the following :	
		(i) SIM	(5)
		(ii) RIM	(5)
IX.	(a)	Explain the instruction set of 8085.	(10)
	(b)	Explain the various addressing modes available in 8085.	(10)
		OR	
X.	(a)	Draw the timing diagram for the execution of the instruction MVI A, 32H and explain it.	(12)
	(b)	Differentiate between memory mapped I/O and I/O mapped I/O.	(8)

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