3E2075

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B.Tech. IIIrd Semester (Main/Back) Scheme Examination, Feb. - 2011

Computer Engineering & Information Technology

3IT5 & 3CS5 Digital Electronics

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt overall **five** questions, selecting **one** question from **each** unit. Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly.*

Unit - I

1. a) Convert the decimal number 250.5 to base 3, base 4 and base 7. **(6)**

   b) Find the 10's complement of $(935)_{11}$. **(2)**

   c) Find the equivalent Gray Code for $(478)_{10}$. **(2)**

   d) Obtain the weighted binary code for base - 10 digits using weights of 5421. **(2)**

   e) Find the complement of the following boolean functions by finding dual of them :

      i) $F(A,B,C) = (A+B'+C)(A+B')(B+C')(A+B+C)$.

      ii) $F(w,x,y,z) = y'z + wxy' + wxz' + w'x'z$. **(4)**

OR

   a) Represent the decimal number 2047 as

      i) Radix - 2 number

      ii) BCD code

      iii) 8, 4, -2, -1 code

      iv) Excess -3 code **(4)**

   b) Represent $(-17)_{10}$ in

      i) Sign Magnitude form

      ii) 1's complement representation **(2)**

   c) Find the radix '*r*' for the following equations to be valid :

      i) $\sqrt{71} = 8$

      ii) $\frac{53}{3} = 15$ **(4)**

d) Perform the following :

i) $(72532)_{10} - (3250)_{10}$ 10's complement subtraction.

ii) $(28)_{10} + (95)_{10}$ BCD Addition.

iii) $(74)_8 - (35)_8$ 7's Complement subtraction. **(6)**

Unit - II

2. a) Explain the functioning of following gates using appropriate circuit - diagram:

i) CMOS NAND Gate

ii) CMOS NOR Gate **(6)**

b) Tabulate the comparison between different logic families on the basis of their typical characteristics. **(6)**

c) Write a short note on :

'Propagation Delay in Digital logic gates'. **(4)**

OR

a) Explain the functioning of following gates using appropriate circuit - diagram:

i) TTL Gate with open - collector.

ii) TTL Gate with Totem - pole output. **(8)**

b) Explain the function performed by the wired - OR gate with its circuit diagram. **(4)**

c) Explain the following :

i) Power Dissipation

ii) Noise Margin **(4)**

Unit - III

3. a) Simplify the boolean function by using quine - McCluskey method :

$F(A, B, C, D) = \sum_m (1, 3, 7, 11, 15) + d\ (0, 2, 5)$. **(8)**

b) Simplify the following boolean function using K-map and give simplified expression in SOP form :

$F\ (A, B, C, D) = \Pi\ (0, 1, 2, 3, 4, 10, 11)$ **(4)**

c) Minimize the following expressions by using the basic laws of boolean algebra:

i) $Y = AB + \overline{AC} + A\overline{B}C(AB + C)$

ii) $Y = \overline{A}BC + \overline{B}CD + AC + \overline{A}\,\overline{B}\,C\overline{D}$ **(4)**

OR

a) The following boolean expression **(6)**

$F = Z(w' + y)$

is a simplified version of the expression

$F = (w' + y)(x' + z)(w' + z)$

Find the don't care conditions, if any.

b) Simplify the following boolean function, using the don't care conditions *d,* with K-map and realize the simplified expression with NOR gates only. **(8)**

$F = A'B'D' + A'CD + A'BC$
$d = A'BC'D + ACD + AB'D'$

c) Express the function

$F = A + \overline{B}C$ **(2)**

i) in canonical SOP form

ii) in canonical POS form.

Unit - IV

4. a) Design a 4-bit parallel ADDER/SUBTRACTOR circuit with ADD/SUB control line. **(6)**

b) Design and implement a Full-Subtractor circuit using 3-to-8 decoder and external gates. **(4)**

c) Design and implement a combinational circuit for addition of two one-digit BCD numbers. **(6)**

OR

a) Implement the following function using a multiplexer having two select lines A and B.

$F(A, B, C, D) = \sum_m (1, 3, 5, 6, 9, 11, 13, 15)$. **(6)**

b) Construct a 5×32 decoder with four 3×8 decoders and a 2×4 decoder. **(6)**

c) For three - inputs, prove that Exclusive - OR function and Equivalence function, both are same. **(4)**

Unit - V

5. a) Design a Synchronous counter using D-flip flops for the following binary sequence :

0, 1, 3, 7, 6, 4 and repeat. **(8)**

b) Design a 4 - bit, Mode - controlled Bidirectional shift register using SR flip flops and explain its working in both directions. **(8)**

OR

a) Design an asynchronous Decade Counter. Explain the steps of designing and draw its state diagram also. **(8)**

b) Reduce the state - table given below and draw the state - diagram for reduced table. **(4)**

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

c) Derive the state-table and state-diagram of the sequential circuit of the figure given below. What is the function of the circuit. **(4)**