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B. Tech
BCSE 3307

Sixth Semester Examination – 2008

COMPUTER ARCHITECTURE AND ORGANIZATION – II

Full Marks – 70

Time : 3 Hours

*Answer Question No. 1 which is compulsory
and any **five** from the rest.*

*The figures in the right-hand margin
indicate marks.*

1. Answer the following questions : 2×10
- (a) Why GPR based machines are most widely used ?
 - (b) Differentiate between RISC and CISC machines.
 - (c) What do you understand by quantitative principle of computer design ?
 - (d) What do you mean by interleaved memory organization ?

P.T.O.

- (e) Why does pipelining improve performance ?
- (f) Why does increasing the capacity and associating of a cache generally tend to increase its hit rate ?
- (g) What is the use of pipeline reservation tables ?
- (h) List down various instruction hazards.
- (i) Write at least four differences between a multiprocessor and multicomputer system.
- (j) Why the performance of a parallel computer is improved by using a two level cache memory ?

2. Derive expressions for the three different performance measures of a pipelined unit in terms of the number of stages k , number of jobs/tasks n , and the pipeline cycle time T . Compute each of these measures for a 4-stage pipeline having delays of 15ns, 25ns, 45ns, and 30ns in the different stages while processing 100 jobs. Assume a latch delay of 5 ns. 10

- 3. (a) What is an Illiac recirculating network ? How it is different from barrel shifter ? Explain. 4
- (b) Answer the following with respect to Illiac and barrel shifter network assuming 16 PEs in each : 6
 - (i) Find the number of nearest neighbors in each of the networks.
 - (ii) What is the condition for which both the networks are identical ?

- 4. (a) What are the different pipeline hazards ? How do they affect the speedup ? 5
- (b) Identify the data hazards while executing the following instruction in DLX pipeline. Draw the forwarding path to avoid the hazard. 5

```
ADD R1, R2, R3
SUB R4, R1, R5
AND R6, R1, R7
OR R8, R1, R9
XOR R10, R1, R11
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- 5. (a) What are the different techniques adopted to reduce miss penalty ? 5
- (b) What are vector length and vector stride ? Explain with example. 5

6. What kind of parallelism is exploited in each of the following parallel architectures ? 10

- (i) Pipeline Computers
- (ii) Array Processors
- (iii) MIMD Architectures.

7. How do tightly coupled system differs from loosely coupled ones ? Explain how intra and interprocessor communication take place in a non-hierarchical loosely coupled system ? 10

8. (a) Represent the following program segment in the form of a data flow graph : 5

For i = 1 to m do

begin

c(i) = 0

For j = 1 to n do

c(i) = c(i) + a(i, h)*b(j)

end.

(b) Explain the advantages of dynamic DFCs over static DFCs. 5