Fifth Semester Examination – 2008

MICROPROCESSOR AND MICRO CONTROLLER

Full Marks – 70

Time : 3 Hours

Answer Question No. **1** which is compulsory
and any **five** from the rest.

The figures in the right-hand margin
indicate marks.

1. Answer the following questions :   2 × 10

   (a) How many bytes are addressable the 8086 ?

   (b) In 8086 which register holds the address of the next instruction.

   (c) List all the segment register and Index registers in 8086.

P.T.O.

(d) Why are memory segments limited to 64K?

(e) What determines the address of the 1st instruction in memory?

(f) Explain why CS can be source but cannot be a destination.

(g) What are packed and unpacked BCD numbers?

(h) Give the address locations of RAM assigned to various register banks in 8051 microprocessor.

(i) Write an instruction in 8086 that will move the immediate value 1234H into the CX register. Which type of addressing mode is it?

(j) In 8086 how is minimum and maximum mode of operation are selected?

2. (a) What are the different addressing modes in 8086? Explain with examples. 7

(b) How does a logical address differ from a physical address in 8086?   3

3. Write an assembly language program with a flow chart for addition of a three byte number that is stored at address 600003 H to the three byte number that is double word stored at address 60000 H and store the result at address 600020 H to 600203 H.   10

4. Write an assembly language program for 8051 microprocessor to copy the value 55H into RAM memory locations 40 H to 45 H using   10

(a) Direct addressing mode

(b) Register indirect addressing mode without a loop

(c) With a loop.

5. (a) Explain the organization of 8085 CPU with a neat sketch.   6

(b) Show by a suitable figure how the low order byte of the address is latched and also state why it is latched?   4

6. Show the memory map to obtain $4K \times 4$ memory using the following chips.   10

  (a) $1K \times 4$ RAM

  (b)   2 line to 4 line decoder.

7. Explain how segment register is combined with an offset in 8086 and the concepts of physical and logical memory in 8086.   10

8. (a)   Explain the functions of BIU and EU in 8086.   7

  (b)   What would be the offset required to map to physical address location $002C3_{16}$ if the contents of the corresponding segment register are $002A_{16}$?   3

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