THIRD SEMESTER B.E. DEGREE MAKEUP EXAMINATIONS - JANUARY 2007 SUBJECT: ELECTRONIC DEVICES \& CIRCUITS (BME 201 ) (REVISED CREDIT SYSTEM)
Friday, January 05, 2007: 9.00 a.m.- 12.00 noon
TIME: 3 HOURS
MAX. MARKS: 100

## Instructions to Candidates:

1. Answer any FIVE full questions.
2. Draw labeled diagram wherever necessary
3. (a) With a neat diagram explain junction behavior of diode 08
(b) Explain various current components of diode 06
(c) Explain working principle of Zener diode and list its applications.

06
2. (a) Write short notes on:
(i) UJT ,
(ii) LED
(b) Draw a neat diagram of n-channel type JFET. Explain its operation with drain and transfer characteristics.
3. (a) Explain how phototransistor is different than BJT. List its two ..... 06 applications
(b) What is photolithography? Explain various steps in the fabrication ..... 08 of Integrated Circuits.
(c) Write an ac equivalent model of JFET in fixed biased ..... 06
configuration. Calculate $\mathrm{Zi}, \mathrm{Zo}$ and Av (with and without effect of rd)
4. (a) Draw the circuit of a common base npn-transistor. Plot the input ..... 08 and output characteristics and explain
(b) For the circuit shown in the fig Q.4b, transistors Q1 and Q2 ..... 08 operate in the active region with $\mathrm{V}_{\mathrm{BE} 1}=\mathrm{V}_{\mathrm{BE} 2}=0.7 \mathrm{~V}, \beta 1=100$, $\beta 2=50, \mathrm{I}_{\mathrm{CO}}=0$. Find $\mathrm{I}_{\mathrm{B} 2}, \mathrm{I}_{1}, \mathrm{I}_{2}, \mathrm{I}_{\mathrm{C} 2}, \mathrm{I}_{\mathrm{B} 1}, \mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{E} 1}, \mathrm{vo}_{1}, \mathrm{vo}_{2}$.
(c) Discuss on cutoff region of a transistor ..... 04
5. (a) Discuss on fixed bias and thermal stabilization of transistor ..... 07
(b) A Ge transistor is used in the self biasing arrangement with $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V}, \mathrm{R}_{\mathrm{C}}=1.5 \mathrm{~K}$ and $\mathrm{V}_{\mathrm{BE}}$ active $=0.2 \mathrm{~V}$. The quiescent point is chosen to be $\mathrm{V}_{\mathrm{CE}}=8 \mathrm{~V}$ and $\mathrm{I}_{\mathrm{C}}=4 \mathrm{~mA}$.A stability factor $\mathrm{S}=12$ is desired .If $\beta=50$, find $R_{1}, R_{2}$ and $R_{E}$
(c) Draw the hybrid- $\pi$ model of a npn transistor in the CE configuration. Discuss on the circuit components
6. (a) For the amplifier shown in the fig Q.6a, compute $\mathrm{A}_{\mathrm{I}}=\mathrm{Io} / \mathrm{II}, \mathrm{Av}, 08$ Avs, Ri, and $\mathrm{Ri}^{1}$. Given hfe $=50$,hie $=1.1 \mathrm{~K}$, hre $=$ hoe $=0$.
(b) Discuss on :
(i) High input impedance buffer amplifier
(ii) Bias compensation circuits


