B.TECH DEGREE EXAMINATION MAY/JUNE 2009

Eighth Semester

Branch: Applied Electronics and Instrumentation, Electronics and Instrumentation, Electronics and Communication Engineering

ADVANCED MICROPROCESSORS (ASL)

(Regular/Supplementary)

Each question carries 4 marks.

1. What is meant by minimum and maximum mode of operation of 8086 processor?
2. How Physical address is generated in 8086?
3. Discuss any four data addressing modes with examples.
4. Define Stack. What are stack addressing modes?
5. List the salient features of 80286 processor.
6. What is meant by protected mode of operation?
7. Discuss the memory segmentation and virtual memory in 80386.
8. Explain the task switching in 80386.
9. Explain superscalar architecture of Pentium.
10. Explain the features of RISC architecture.

Each question carries 12 marks.

11. With a neat block diagram, explain the architecture of 8086 processor. Explain clearly how pipelining is incorporated in the architecture.

Or

12. (a) Discuss the interfacing and communication between 8086 and 8087.
    (b) Explain the 8086 memory organisation. Discuss the even and odd memory banks.

13. (a) Discuss the program memory addressing modes of 8086 with examples.
    (b) Explain the physical address formation in different addressing modes.

Or

14. Explain the following data addressing modes with examples:-
    (i) Index addressing. (ii) Scaled addressing.
    (iii) Direct addressing. (iv) Indirect addressing.

15. (a) Explain the concept of virtual memory.
    (b) Explain the physical address formation in real mode and protected virtual address mode operation in 80286.

Or

16. (a) Discuss the register organisation of 80286.
    (b) Draw and explain the structure of a general 80286 descriptor.

17. With a neat block diagram, discuss the internal architecture of 80386 processor.

Or

18. (a) Discuss the paging mechanism of 80386 in detail.
    (b) What are the different exceptions generated by 80386?

19. (a) What are the major architectural advancement in 80486 over 80386 ?
    (b) Explain the five stage instruction pipeline.

Or

20. Write short notes on the following:-
    (a) Branch prediction logic.
    (b) BIST (Built In Self Test).
    (c) MMX technology.