G 6140 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY/JUNE 2009

Eighth Semester

Branch : Electronics and Communication Engineering / Applied Electronics and Instrumentation Engineering

VHDL (Elective-II) (L, A)

(Regular/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 4 *marks.*

1. What is VHDL?
2. Explain with an example how an entity is declared.
3. What are the contents of the architecture body in behavioural modelling?
4. Discuss the syntax of conditional signal assignment statement.
5. What is component instantiation?
6. Why configurations are needed?
7. Describe the format of a subprogram body.
8. Explain the syntax of a package body.
9. What is an alias? Explain with an example.
10. Explain the methods of generating stimulus values.

(10 × 4 = 40 marks)

Part B

Each question carries 12 *marks.*

11. Explain with examples the scalar types used in VHDL.

Or

12. Explain the operators used in VHDL.

Turn over

13. Obtain a behavioural model of a 10 bit synchronous counter.

Or

14. Write a VHDL model of an *n*-bit parallel to serial converter.

15. Describe the structural model of an 8-bit parity generator.

Or

16. Write a note on conversion functions.

17. Explain with examples, subprogram overloading.

Or

18. Explain how compiled design units are stored in design libraries.

19. Describe the different classes of predefined attributes.

Or

20. Discuss the methods of modelling synchronous logic.

(5 × 12 = 60 mar