ET3004

III Semester B.TECH in Electronics & Tele Communication Engg. Examinations, August 2011

DIGITAL ELECTRONICS

Time: 3Hours Max. Marks: 75

Instruction: *Answer* ***any FIVE*** *questions from* ***Part-A,*** *and* ***Part-B***

PART –A

I. Answer any five questions: (5 X 5 = 25)

1. Perform the subtraction of 3-7 using 1's complement.
2. Explain the four types of connection.
3. Explain the propagation delay of a gate.
4. Write the differences between positive and negative logic gates.
5. Discuss about memory address decoder.
6. Explain briefly about PLA.
7. Illustrate pulse mode asynchronous circuit.
8. Draw the diagram of 16 X 8 bit ROM

PART -B

I. Answer any five questions: (5 X10= 50)

9. Convert the following decimal numbers to their hexadecimal equivalent (i) 14_{10} (ii) 80_{10} (iii) 3000_{10} (iv) 62.500_{10}.
10. Write the steps for simplifying a logic expression using a Karnaugh map.
11. Enumerate the precautionary measures to be considered while handling CMOS device.
12. Give an account on multilevel gates.
13. Implement the expression (i) AB + BCD + EFGH (ii) (A+B) (C+D+E) (F+G+H+I).
14. Draw the logic diagram for a master level salve J-K flip flop and explain.
15. Draw the fundamental mode asynchronous circuit and explain in detail.
16. Elaborate the single fused PROM cell with clear sketch.