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MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL
(A Constituent Institute of Manipal University, Manipal)

THIRD SEMESTER B.E. DEGREE END SEMESTER EXAMINATION
(REVISED CREDIT SYSTEM)

11 December 2010

ANALOG ELECTRONIC CIRCUITS (ELE 209)

Time: 3 hours **Max. Marks: 50**

Note : Answer any **FIVE** full questions. Refer Table-1 for h-parameters.

1A. Determine V_0 for the circuit shown in Fig 1(A). (02)
1B. Define Transition time, storage time and reverse recovery time with respect to a PN junction diode (03)
1C. Plot the waveform by determining V_0 for the circuit shown in Fig 1(C). (05)

2A. Determine the transistor quiescent voltages and currents of the amplifier shown in Fig 2(A). Assume V_{BE}=0.7V. (03)
2B. From the fundamental derive an expression for $S(I_{CBO})$, for voltage divider biasing circuit with emitter resistance R_E. (04)
2C. Draw the small signal h- parameter model of a Darlington pair transistor connection. Hence list out its merits and demerits. (03)

3A. Design a voltage divider biasing circuit to meet the following specifications, V_{cc}=25V, V_{CE}=4V, I_C=10mA, $\beta = 100$, $S \leq 5$ and R_E=100Ω. Hence draw the circuit. (05)
3B. For the cascaded amplifier shown in Fig 3(B) determine A_V, $A_{VS} = v_0/v_S$, and R_i using approximate h-parameter transistor model. (05)

4A. An NMOS has $V_t = 0.5V$ and $\frac{W}{L} = 10$, $\mu_n C_{ox} = 200\ \mu A/v^2$. Determine
  i. The value of the V_{GS} to operate in saturation region with a dc current I_{DC}=100mA.
  ii. Value of the V_{GS} required to cause the device to operate 1000Ω resistor for very small ac, v_{DS} signal. (02)
4B. The MOSFET shown in Fig. 4(B) has $\mu_n C_{ox} \frac{W}{L} = 0.4mA/V^2$, V_t=1V, r_0=40K. Determine all the quiescent current and voltages and hence determine the output voltage when sinusoidal v_i=0.8mv is applied at the input of the amplifier. (04)
4C. Derive an expression for current gain, the input resistance and output resistance of a single common gate MOSFET amplifier (04)

5A. In the amplifier shown in the circuit Fig. 5(A), both the MOSFETs are having V_T=0.7V, $\mu_{n1} C_{ox1} = \mu_{n2} C_{ox2} = 500\mu A/V^2$, aspect ratio of MOSFET M1=$\frac{W_1}{L_1} = 100$ and the drain current of MOSFET M2 =I_{D2}=2mA. Determine
  i. The quiescent V_{GS} and V_{DS} of both the MOSFETs and aspect ratio $\left(\frac{W_2}{L_2}\right)$ of M2
  ii. Draw the small signal equivalent circuit and hence find small signal voltage gain from v_s to v_o.
  iii. Maximum sinusoidal input that can be applied before the output begin to clip. (06)
5B. For a transformer coupled class A power amplifier, derive an expression for efficiency and hence obtain maximum efficiency. Also list any two disadvantages of the same. (04)

6A. Determine the lower and upper cut off frequency of the CE amplifier shown in Fig 6(A). Hence find the band width. Assume the R_0=50K, C_1=1µF, C_2=4µF, C_0=1nf and C_E=10µF. (04)
6B. Determine the output voltage V_0, V_{CE} and currents through all the resistance in the circuit shown in Fig. 6(B), where V_{BE} = 0.7 V (04)
6C. Design a 7805 variable voltage regulator to get an Output voltage range 6V to 16V. Take R_1 = 1K, I_{adj}=4.3mA. Draw the circuit. (02)

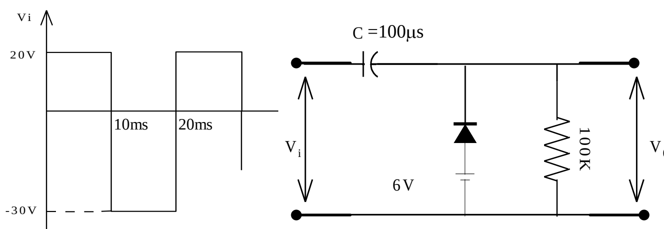

Fig 1(A)

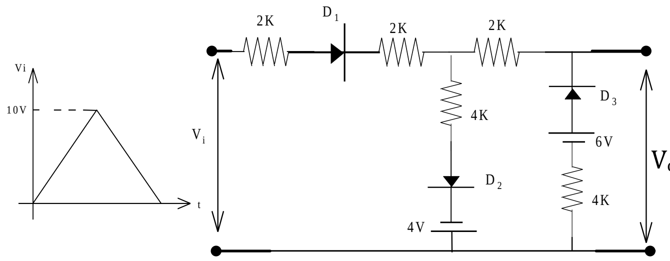

Fig 1(C)

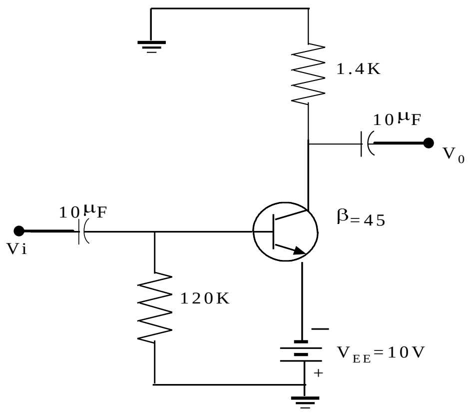

Fig 2(A)

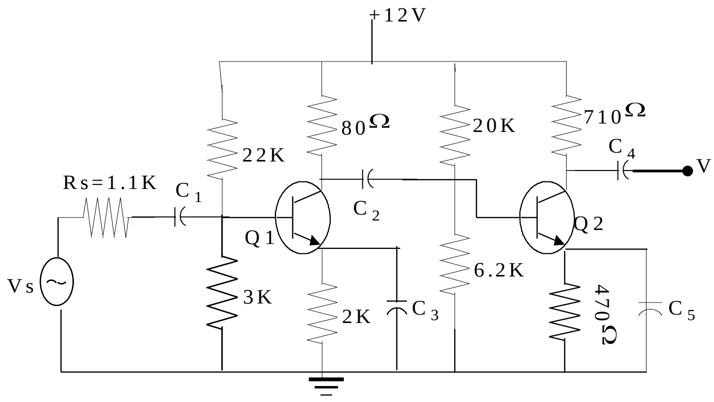

Fig 3(B)

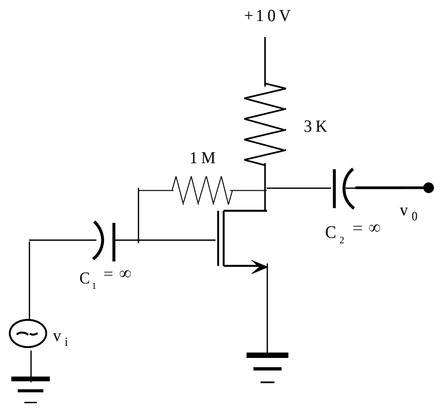

Fig 4(B)

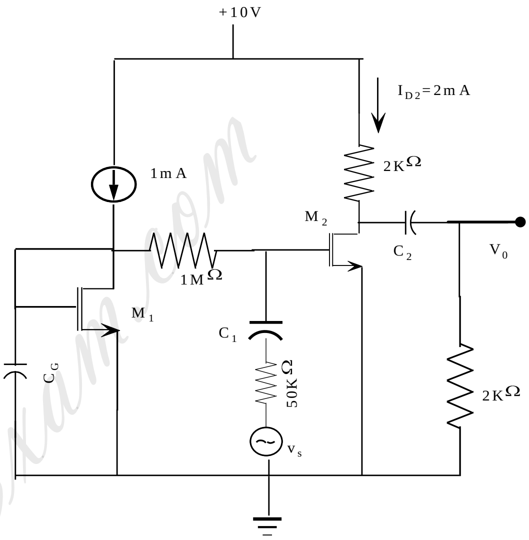

Fig 5(A)

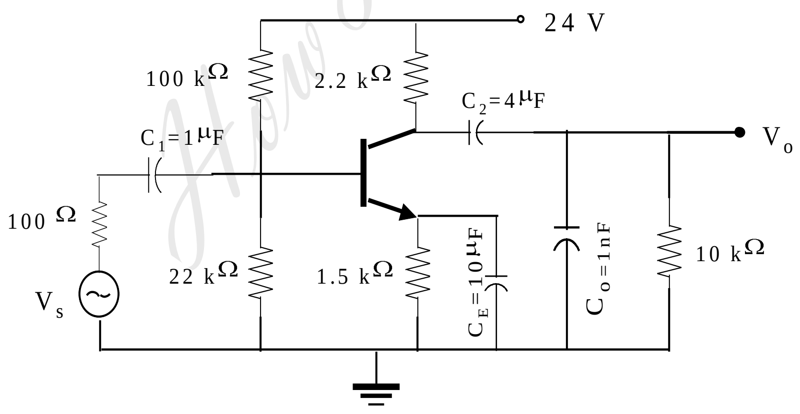

Fig 6(A)

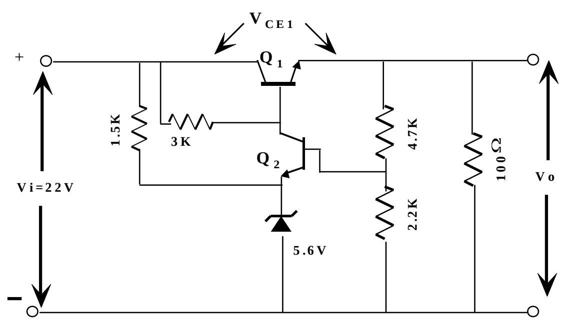

Fig. 6(B)

Table-1

h-parameters	CE	CB	CC
h_i	1.1K	1.1K	21.6 ohms
h_r	2.5×10^{-4}	1	2.9×10^{-4}
h_f	50	-51	-0.98
h_o	24μmho	25μmho	0.49μmho