D 1094 (Pages : 2) Name.....

Reg. No.....

EIGHTH SEMESTER B.TECH (ENGINEERING) DEGREE EXAMINATION

DECEMBER 2009

CS 04 802 : COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

1. (a) Discuss the measuring performance.
   (b) Write short notes on addressing modes.
   (c) What is meant by Instruction level parallelism ? Explain.
   (d) Explain the vector architecture with neat diagram.
   (e) Distinguish between Cache memory and Virtual memory.
   (f) How will you improve the cache performance ?
   (g) What are the characteristics of Application domains ?
   (h) Discuss connection oriented and connectionless communication.

(8 × 5 = 40 marks)

Part B

Module I

2. (a) (i) How are Instruction set architecture classified ? Explain.
   (ii) Explain addressing modes for signal processing with example.

Or

(b) Discuss the DLX architecture and what is the major limitation in simple pipelining technique.

Module II

3. (a) Explain dynamic scheduling using Tomasulo's approach with necessary diagram and give example.

Or

(b) (i) Describe the limitations of Instruction Level Parallelism.
   (ii) Explain the vector processing principle.

Turn over

Module III

4. (a) (i) Discuss different miss rate reduction technique.

(ii) Discuss the techniques for improving the performance of main memory.

Or

(b) (i) Explain virtual memory in detail.

(ii) Discuss the UNIX file system performance.

Module IV

5. (a) (i) Discuss in detail about a simple network with necessary diagrams.

(ii) Discuss the performance parameters of interconnection networks.

Or

(b) Explain the practical issues for commercial Interconnection networks.

(4 × 15 = 60 marks)