Sub. Code: 2961

2118

B. E. (I. T) 3rd Semester

IT-315 Digital Electronics

Time Allowed: 3 Hours Max. Marks: 100

Note: Attempt any five questions, selecting atleast two questions from each Part A and Part-B.

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PART-A

I (a) Express the following nos. in decimal: $(10110.0101)_2$, $(16.5)_{16}$ and $(26.24)_8$.

(b) The solution to the quadratic equation $x^2-11x+22=0$ is $x=3$ and $x=6$. What is the base of the numbers?

(c) Convert the hexadecimal no. 68BE to binary and then from binary, convert it to actual.

(d) Represent decimal no. 6027 in (i) BCD (ii) Excess-3 code (iii) 2421 code. (6,4,4,6)

II (a) Define Positive and Negative logic. Represent universal gates with help of it . How is De-Morgan's theorem related to it? Also convert NAND to EX-OR gate using minimum no. of gates.

(b) Implement $F(A,B,C,D) = \Sigma(1,3,4,11,12,13,14)$ using a 8:1 MUX.

(c) Design a BCD-to-7-segment decoder. (6,6,8)

III (a) Using 10's complement, subtract 3250-72532.

(b) Simplify using Boolean algebra only:-

$F=X\bar{Y}Z+\bar{X}\bar{Y}Z+\bar{W}XY+W\bar{X}Y+WX\bar{Y}$.

Also obtain truth table and draw logic diagram using simplified expression. (8,12)

IV (a) Design a counter with the following repeated binary sequence: 0,1,2,3,4,5,6. Use J-K flipflops.

(b) What is the difference between serial & parallel transfer? Explain how to convert serial data to parallel and parallel data to serial, what type of register is needed? (10,10)

P.T.O.

PART-B

V (a) Design a combinational circuit using a ROM. The Ckt. accepts a 3-bit number and generates an output binary no. equal to the square of the input number.

(b) Draw and explain the circuit diagram for a 16-bit ROM array using diode matrix coufig.. (10,10)

VI The following are the specifications for the schottky TTL 74500 quadraple two-input NAND gates. Calculate the fan-out, power dissipation, propagation delay and noise margin of the schottky NAND gate.

Parameter	Name	Value
V_{CC}	Supply voltage	5V
I_{CCH}	High-level supply current	10mA
I_{CCL}	Low-lvel supply current	20mA
V_{OH}	High-level o/p voltage(min)	2.7V
V_{OL}	Low-level o/p voltage(max)	0.5V
V_{IH}	High-level I/P voltage(min)	2V
V_{IL}	Low-level I/P voltage (max)	0.8V
I_{OH}	High-level o/p current(max)	1mA
I_{OL}	Low-level o/p current(max)	20mA
I_{IH}	High-level I/P Current(max)	0.05mA
I_{IL}	Low-level I/P current(max)	2mA
t_{PLH}	Low-to-high delay	3ns
t_{PHL}	High-to-low delay	3ns

(b) Explain with the aid of a circuit diagram, the operation of a standard TTL 3-input NAND gate. What is the function of diode in the path of totem-pole output stage? (8,12)

VII (a) Most DAC's are of either the Binary weighted resistor, or the R-2R type. What are the disadvantages of the former and when might it be employed?

(b) What are the various processes, followed in an ordered sequence for converting an analog signal to a digital form? How can quantization error be reduced? (10,10)

VIII Write short notes on the following:-

(a) Tristate Logic

(b) Flash type ADC

(c) CMOS Inverter.

(d) Reading operation in RAM (4x5)