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Thapar Institute of Engineering & Technology, Patiala
Computer Science & Engineering Department
M.E. (Computer Sc.) 1st Year 1st Semester
End Semester Test

Course Code: CT-002 Date: 13/12/06
Course Name: Advanced Computer Architecture Time Allowed: 3 Hr.
Instructor: Shalini Batra Max. Marks: 45

Note : Make suitable assumptions ,if required, **with reasoning**

Q1.a) Given below is a reservation table with four stages

	0	1	2	3	4	5	6	7
S1	X							X
S2		X	X					
S3				X	X		X	
S4						X	X	

a) List the set of forbidden latencies between task initiations. (1)
b) Give the collision vector C . (1)
c) Draw the state diagram which shows all possible latency cycles. (2)
d) List all simple cycles from the state diagram. (1)
e) List all greedy cycles from the state diagram. (1)
f) Determine the minimal average latency (MAL). (1)

b) Explain static and dynamic pipeline. (2)

Q2.a) Draw a 8 X 8 Omega network (3)

b) Let's assume that we have 5-stage pipeline and the time required for the execution of these subtasks is 4 sec., 4 sec.,3-sec., 3 sec., & 2sec. respectively. Can we pipeline these subtasks & enhance the overall performance. If yes, give the space –time diagram for these tasks in a pipeline. (2)

c) Bring out any three important properties of hypercube network (1.5)

d) Explain in detail PE of a array processor. (2.5)

3.a) Diagrammatically represent dynamic coherence check for fetch operation in a multi cache memory organization and explain all four rights in brief. (5)

b) Lets consider a multiprocessor system with private cache has a memory block of 1024 K and L = 16 lines.
Calculate:

1. Modules (N) in each line (1)
2. Words in each module. (1)
3. Minimum length of a block of data for effective memory utilization. (1)
2. If line i and module j be represented by Li and Mj respectively, where would the k^{th} word of the block of data exist on line i. (1)

Q4a) Compare and contrast fork-join and co-begin co-end statements with examples. (4)

b) What are the problems faced in FCFS algorithm in common bus architecture. (2)

c) Depict graphically cost versus no. of processors and performance versus no. of processors for bus, crossbar switch and multistage network. (2)

d) Give one major point of difference between TCS and LCS. (1)

Q5. Write short notes on (3X3)

1. Flynn's and Feng's architectural classification.
2. S-access memory organization .
3. Multi-stage Networks.