END SEMESTER EXAMINATION, Dec 2006
M TECH 2nd year (VLSI and EIC)
Subject: ASIC and FPGAs (VL016)
Thapar Institute of Engineering and Technology, Patiala

Time allowed : 3 hrs **Max. Marks : 60**

Attempt any six questions out of eight questions
Attempt parts of the same question in sequence
Illustrate with suitable diagrams wherever required
See your answer sheets on 12 Dec,2006 at 11.00 AM in my office

1.Q a) Explain in detail the basic ATPG algorithm. Illustrate with the help of example? (4)
b) Explain a two input CMOS NAND Gate? (3)
c) Find the capacitances in all operating modes for PMOS device with $t_{OX} = 22A^{\circ}$. Device dimensions are W=400nm and L=100nm. $\varepsilon_{ox} = 35.4 \times 10^{-14}$ F/cm. Neglect lateral diffusion. (3)

2.Q a) Explain the following technologies for programmable ASICs
i) Antifuse ii) SRAM iii) EEPROM (3+3+3)
b) Define the term ASIC? (1)

3.Q a) What are packages and libraries in VHDL? (2)
b) Write a dataflow architecture for half adder in VHDL? (2)
c) Write a VHDL code for 8 bit ripple carry adder. Draw the block diagram in support of the code. (6)

4.Q a) Explain boundary scan test with respect to the following points
i) JTAG ii) TAP iii) TAP controller iv) Bypass Register (1+2+3+2)
b) Explain Metastability. (2)

5.Q a) Explain the interconnect architecture of any one of the following
i) ACTEL FPGA ii) XILINX FPGA (5)
b) Explain Gate Array based ASICs? (5)

6.Q a) Design a 16x1 single port edge triggered RAM using XILINX XC 4000 FPGA. Explain the timing diagram also. (5)
b) What are the different types of I/O requirements in ASICs? (3)
c) What is a cell library in low level design entry? (2)

7.Q Write short notes on
i) Logic Synthesis ii) Supply Bounce (5+5)

8.Q a) Explain programmable ASIC logic cell of any one of the following
i) ACTEL ii) XILINX iii) ALTERA (5)
b) Explain the different types of simulation? (5)