THAPAR INSTITUTE OF ENGINNREING AND TECHNOLOGY
PATIALA
ME 2ND YEAR (VLSI)
DEPARTMENT OF ELECTRONICS
END SEMESTER EXAMINATION

Course Code: VL025
Course Name: VLSI Architecture
Instructor: Paramjit Kaur

Time Allotted:3hrs
Max Marks: 45
Date: 7th Dec, 2006

NOTE: Q 1 is Compulsory. Do any three questions from Q2 to Q6.

Q1 Discuss (3X5)

a) Procedure Calls of RISC
b) Register Window of RISC
c) Pipelining Hazards
d) Optimization of Pipelining
e) RISC vs. CISC
f) Superscalar vs. Super pipelining

Q2. Explain Motorola 88000, including Register Management, Instruction Unit pipeline with diagram? (10)

Q3. (a) Mention the limitations of Superscalar Approach? (2X5)
(b) Mention the design issues of Super scalars?

Q4. Explain the PowerPC 601 with block diagram including Dispatch Unit, Instruction Pipeline? (10)

Q5. Explain the classification of Pipeline Processors?
(a) Instruction
(b) Arithmetic (10)

Q6. Explain the characteristics and functions of CISC and its comparison with CISC?(10)