END SEMESTER EXAM.

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Thapar Institute of Engineering and Technology, Patiala

HDL Based Digital Design (EC-020)

B.E. Final Year

Time: 3Hours **Max Marks.: 36**

Note: Questions 1 to 4 are compulsory. Attempt any one question from 5 and 6.

Q1(a) Write a variable declaration for a counter, initialize to zero. **(2)**

(b) Write a case statement that strips the strength information from a standard logic variable x. If x is '0' or '1' set it to '0'. If x is '1' or 'h' set it to '1'. If x is 'X', 'w', 'z', 'U' or '_', set it to 'x'. **(4)**

Q2(a) What does decimal numbers are represented by the following literals: **(3)**
2#1000_0100# 2#1E15

(b) Write a wait statement that suspends a process until a signal changes from '1' to '0' while an enable signal s1. **(3)**

(c) Implement a BCD to Excess-3 decoder using PLA's. **(4)**

Q3(a) What is operator overloading? Give example. **(3)**

(b) Give all the type and range attributes and explain. **(3)**

Q4(a) Write the package declaration that defines the subtype of natural numbers representable in eight bits and a component declaration for an adder that adds values of subtypes. **(5)**

(b) Give an example of type conversion and syntax for alias declaration. **(2+1)**

Q5(a) Write a loop statement that samples a bit input d when a clock input clk changes to 1 so long as d is 0, the loop continues executing. When d is 1, the loop exits. **(3)**

(b) Write a declaration for a function that tests whether an integer is odd, as the function declaration would appear in package declaration. **(3)**

Q6(a) How would you write a full test bench. Explain. **(5)**

(b) Write a declaration for a subtype of std_ulogic_vector, representing a byte. Declare a constant of this subtype with each element having the value Z. **(1)**