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THAPAR INSTITUTE OF ENGINEERING AND TECHNOLOGY, PATIALA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC- 027 VLSI CIRCUIT DESIGN (B.E. V^{th} Sem EC) [4.12.2006]

TIME: 3 HOURS **END SEMESTER TEST** **MAX.MARKS:45**

Instructor: Balwant Singh

Note: ***1. Attempt ANY FIVE Questions Sequentially.***
2. Graph sheets may be asked for, if required.
3. All questions carry equal marks.
4. Make reasonable assumptions for missing information, if any.

Q I a) Describe the structure of an n-channel enhancement type MOSFET. What do you understand by flat band voltage? Explain

b) Find the threshold voltage and body factor γ for an n-channel transistor with an n^+ silicon gate if $t_{ox} = 200$ A°, $N_A = 3 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 4 \times 10^{19}$ cm^{-3}, and if the number of positively charged ions at the oxide-silicon interface per area is 10^{10} cm^{-2}. (3, 6)

Q II a) Draw and explain the energy band diagrams of:

i) The combined MOS system.

ii) The MOS structure operating in depletion mode under small gate bias.

b) Consider a process technology for which $L_{min} = 0.4$ µm, $t_{ox} = 8$nm, $\mu_n = 450$ cm^2/Vs , and $V_t = 0.7$ V.

(i) Find C_{ox} and K_n'.

(ii) For a MOSFET with W/L = 8 µm/0.8µm, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in saturation region with a DC current $I_D = 100$ µA.

(iii) For the device in (ii), find the value of V_{GS} required to cause the device to operate as a 1000 Ω resistor for very small v_{DS}. (3, 6)

Q III a) Discuss with neat labeled diagrams, how an inverter is fabricated in a p-well CMOS process.

b) For a CMOS –2 input NOR gate, draw

i) Circuit diagram ii) typical layout (5, 4)

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Q IV a) Explain the time domain behavior of a CMOS bistable element along with a circuit diagram.

b) Draw CMOS SR latch circuit based on NOR 2 gates. Give truth table and explain the circuit operation.

c) What is scaling? Describe with the help of examples, different scaling techniques. (3, 3, 3)

Q V a) Discuss physical origin of latch up and give latch up prevention techniques.

b) What are the components of power dissipation in CMOS circuits? Explain in detail.

c) What do you understand by dynamic CMOS Logic? Describe basic CMOS dynamic gate circuit operation.

d) What are BiCMOS circuits? Describe. (3, 3, 2, 1)

Q VI a) Draw a basic resistive load inverter circuit. Derive expressions for all the critical point voltages and explain typical VTC of a resistive load inverter circuit.

b) Calculate t_f, t_{pHL}, t_r & t_{pLH} for the symmetric CMOS inverter.

V_{DD} =5V ; k'_n= 40μA/V^2,$(W/L)_N$= 4μm/2μm

Vtn=1V; k'_p=16μA/V^2,$(W/L)_P$= 8μm/2μm Vtp= -1V.

Use a load Capacitance of 0.1pF. (5, 4)

Q VII a) Find the depletion region width $\mathbf{x_d}$, the depletion region charge $\mathbf{Q_{BO}}$,threshold voltage with no source to body voltage $\mathbf{V_{THO}}$, and body factor γ of a device with following physical parameters

t_{ox} = 400 A°; N_A = 1.5 x 10^{16} /cm^3 (substrate acceptor doping) ; N_D = 10^{8} /cm^3 (gate donor doping); N_{SS} = 5 x 10^{10} /cm^2(density of singly charged positive surface ions)

b) Calculate the ion implant dose necessary to change the threshold voltage $\mathbf{V_{THO}}$ of the device in (a) above to +1V or to - 4V. Assume 100% ionization of implanted material.

(6, 3)

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