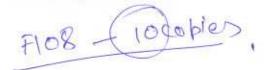
Roll Number:



Thapar University, Patiala. Computer Science & Engineering Department B.E (2nd year COE, EIC)

Course Code: CS004 Date: 11/03/2010
Course Name: Computer System Architecture Time: 2hrs
Instructor: Prateek Bhatia, Karun Verma, Navjot Kaur MM: 30

Note: All the Questions are compulsory and attempt in order. Use of Calculator is not allowed. Draw neat and clean diagrams wherever required.

- a) Design a sequential circuit with two T flip-flops A and B and two 3 inputs E and x. When E=0, the circuit remains in the same state regardless of the value of x. When E=1 and x=1 the sequence is 00,11,10,01,00 and repeat. When E=1 and x=0, the sequence is 00,01,10,11,00 and repeat.
 - b) A computer System has 24 address lines, for a total memory 3 addressability of 2²⁴=16 MB. However, the system needs to be provided with only 2 MB of physical memory, by making use of two memory devices of 1 MB each. The 2MB of memory provided are to occupy the lowest addresses in the total addressable memory of the system. Outline using a circuit diagram how you would decode and make use of the 24 system address lines to achieve this design objective.
- Using 8-bit two's complement integers, perform the following 2 computations
 - i) (-35) + (-11)
 - ii) (19) (-4)
 - Explain with example how BSA and ISZ instruction works.
- Make the following changes to the basic computer.
 Add a register to the bus system CTR (count register) to
 - be selected with S₂S₁S₀=000
 - ii) Replace the ISZ instruction with an instruction that loads a number into CTR

LDC address CTR←M[address]

- iii) Add a register reference instruction ICSZ: increment CTR and skip next instruction if Zero. Discuss the advantage of this change as compared to ISZ.
- b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with input carry C_{in}. Draw the logic diagram for the first two stages.

C _{in} =0	$C_{in}=1$
D=A-1	D=A+B'+1
D=A+B	D=A+1
	D=A-1

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4.

```
AR + PC
Fetch
                            RT.:
                            R'T.:
                                                   IR ← MIARI, PC ← PC + 1
Decode
                           RT,:
                                                   D0, ..., D7 ← Decode IR(12 ~ 14),
                                                                AR ← IR(0 ~ 11), I ← IR(15)
Indirect
                           D,'IT,:
                                                   AR \leftarrow M[AR]
Interrupt
                                                   R ← 1
      T, T, T; (IEN)(FGI + FGO):
                           RT<sub>0</sub>:
RT<sub>1</sub>:
                                                   AR + 0, TR + PC
                                                  M[AR] \leftarrow TR, PC \leftarrow 0

PC \leftarrow PC + 1, IEN \leftarrow 0, R \leftarrow 0, SC \leftarrow 0
                           RT,:
Memory-Reference
   AND
                           D.T.:
                                                  DR ← M[AR]
                          D,T,:
D,T,:
D,T,:
                                                  AC ← AC ∧ DR, SC ← 0
                                                  \begin{array}{l} \mathsf{DR} \leftarrow \mathsf{M}[\mathsf{AR}] \\ \mathsf{AC} \leftarrow \mathsf{AC} + \mathsf{DR}, \, \mathsf{E} \leftarrow \mathsf{C}_{\mathsf{out}}, \, \mathsf{SC} \leftarrow \mathsf{0} \end{array}
   ADD
   LDA
                                                DR - M[AR]
                                                  AC ← DR, SC ← 0
   STA
                                                  M[AR] ← AC, SC ← 0
  BUN
                                                  PC ← AR, SC ← 0
                                                  M[AR] ← PC, AR ← AR + 1
  BSA
                                                  PC ← AR, SC ← 0
  ISZ
                                                  DR - M[AR]
                                                  DR + DR + 1
                                                  M[AR] ← DR, if(DR=0) then (PC ← PC + 1),
                                                  SC ← 0
```

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Design Hardware on Common Bus System for Memory (Read, Write), AR(Increment, Load), PC(Load, Increment)

- 5. a) What is the importance of overflow in Arithmetic Shift operation? 2 How it is detected?
 - Design a common bus system for 16 registers 4-bit each using 2 three state bus buffers.
 - c) Simplify the Boolean function F together with the don't care 2 conditions d in (1) sum of product from and (2) product of sum form

$$F(w, x, y, z) = \Sigma (0, 1, 2, 3, 7, 8, 10)$$

 $d(w, x, y, z) = \Sigma (5, 6, 11, 15)$