F108 + 10 copies.

Roll Number: _____

Thapar University, Patiala.
Computer Science & Engineering Department
B.E (2nd year COE, EIC)

Course Code: CS004 | **Date: 11/03/2010**
Course Name: Computer System Architecture | **Time: 2hrs**
Instructor: Prateek Bhatia, Karun Verma, Navjot Kaur | **MM: 30**

Note: All the Questions are compulsory and attempt in order. Use of Calculator is not allowed. Draw neat and clean diagrams wherever required.

1. a) Design a sequential circuit with two T flip-flops A and B and two inputs E and x. When E=0, the circuit remains in the same state regardless of the value of x. When E=1 and x=1 the sequence is 00,11,10,01,00 and repeat. When E=1 and x=0, the sequence is 00,01,10,11,00 and repeat. 3

   b) A computer System has 24 address lines, for a total memory addressability of 2^{24}=16 MB. However, the system needs to be provided with only 2 MB of physical memory, by making use of two memory devices of 1 MB each. The 2MB of memory provided are to occupy the lowest addresses in the total addressable memory of the system. Outline using a circuit diagram how you would decode and make use of the 24 system address lines to achieve this design objective. 3

2. a) Using 8-bit two's complement integers, perform the following computations 2
   i) (-35) + (-11)
   ii) (19) - (-4)

   b) Explain with example how BSA and ISZ instruction works. 4

3. a) Make the following changes to the basic computer. 3
   i) Add a register to the bus system CTR (count register) to be selected with $S_2S_1S_0$=000
   ii) Replace the ISZ instruction with an instruction that loads a number into CTR
   LDC *address* CTR←M[*address*]
   iii) Add a register reference instruction ICSZ: increment CTR and skip next instruction if Zero. Diseuss the advantage of this change as compared to ISZ.

   b) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with input carry C_{in}. Draw the logic diagram for the first two stages. 3

S	C_{in}=0	C_{in}=1
0	D=A-1	D=A+B'+1
1	D=A+B	D=A+1

261

4. 6

Fetch	$R'T_0$:	AR ← PC
	$R'T_1$:	IR ← M[AR], PC ← PC + 1
Decode	$R'T_2$:	D0, ..., D7 ← Decode IR(12 ~ 14), AR ← IR(0 ~ 11), I ← IR(15)
Indirect	$D_7'IT_3$:	AR ← M[AR]
Interrupt		
	$T_0'T_1'T_2'$(IEN)(FGI + FGO):	R ← 1
	RT_0:	AR ← 0, TR ← PC
	RT_1:	M[AR] ← TR, PC ← 0
	RT_2:	PC ← PC + 1, IEN ← 0, R ← 0, SC ← 0
Memory-Reference		
AND	D_0T_4:	DR ← M[AR]
	D_0T_5:	AC ← AC ∧ DR, SC ← 0
ADD	D_1T_4:	DR ← M[AR]
	D_1T_5:	AC ← AC + DR, E ← C_{out}, SC ← 0
LDA	D_2T_4:	DR ← M[AR]
	D_2T_5:	AC ← DR, SC ← 0
STA	D_3T_4:	M[AR] ← AC, SC ← 0
BUN	D_4T_4:	PC ← AR, SC ← 0
BSA	D_5T_4:	M[AR] ← PC, AR ← AR + 1
	D_5T_5:	PC ← AR, SC ← 0
ISZ	D_6T_4:	DR ← M[AR]
	D_6T_5:	DR ← DR + 1
	D_6T_6:	M[AR] ← DR, if(DR=0) then (PC ← PC + 1), SC ← 0

Design Hardware on Common Bus System for Memory (Read, Write), AR(Increment, Load), PC(Load, Increment)

5. a) What is the importance of overflow in Arithmetic Shift operation? How it is detected? 2

b) Design a common bus system for 16 registers 4-bit each using three state bus buffers. 2

c) Simplify the Boolean function F together with the don't care conditions *d* in (1) sum of product from and (2) product of sum form 2

$$F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$$
$$d(w, x, y, z) = \Sigma(5, 6, 11, 15)$$