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Computer Science and Engineering Department
Thapar Institute of Engineering and Technology

(90)

CS-005 Network System Design
End-Semester Examination 7th December 2006

Time allowed: 3-hr. Max. Marks 36

Instructor: Maninder Singh

Note: a) Question no. 1 is compulsory. b) Attempt any 4 out of remaining 6 questions.

Q1. a) What is the difference between the Workbench and the Transactor?
b) How do you develop code for the StrongARM Core? Give complete details about the tool set and required configurations.
c) Draw IXP1200 block diagram and explain working of each unit in detail.

(1,2,5)

Q2. Discuss the key architectural features of IXP1200. Baseline your comments on the following key issues: Multi-Processing, Distributed Data Storage Architecture, Hardware Multi-Threading, Active Memory Optimization, Concurrency, Block Transfers and Scalability.

(7)

Q3. A Microengine can issue a Reference Command, and then swap out, allowing another thread (within the same Microengine) to run. In this way, while one Microengine thread is waiting for data, or some operation to complete, another thread is allowed to run and complete some useful work. Explain this concept of Context Swapping and Threading in detail with help of neat diagrammatical representations.

(7)

Q4. Trace the sequence of steps a packet travels with in IXP1200, starting from the point when Ethernet MAC receives data.

(7)

Q5. a) Explain the functionality provided by SRAM and SDRAM units.
b) What do you mean by Zero-Overhead when a context switch occurs?
c) List down major application areas where a Network Processor is best suited. Take one example area and layout its design using IXP1200.

(2,2,3)

Q6. a) Figure out the Implementations of Protocol Software possibilities in an application program, in an embedded system and in an operating system kernel.

b) What are various Packet Processing Function which could be performed by a Network Processor? Explain Address Lookup And Packet Forwarding function in detail.

(3,4)

Q7. Write short notes on the following

a) Scratch pad memory b) Explicit Parallelism c) ingress and egress processing

(2,2,3)