THAPAR UNIVERSITY, PATIALA

B.TECH. (DISTANCE EDUCATION) EXAMINATION, SEPTEMBER, 2007

DIGITAL ELECTRONIC CIRCUITS (EE007D)

TIME ALLOWED – 3 hr. MAXIMUM MARKS – 100

NOTE : 1. ALL THE QUESTIONS ARE COMPULSARY.
2. MAKE REASONABLE ASSUMPTION FOR MISSING INFORMATION, IF ANY.

SECTION – A

1 (i) Convert $(6327.4051)_8$ into its equivalent decimal number.
(ii) What is Reflecting code? Give example.
(iii) What are the criteria for the minimization of multiple output switching functions?
(iv) What is a parity bit generator?
(v) What is the difference between edge-triggering and level-triggering?
(vi) Describe the difference between synchronous and asynchronous presetting.
(vii) Define the term "Mask Programmable".
(viii) How are ROMs and RAMs classified?
(ix) Describe what happens to (a) noise margin and (b) switching delay, as V_{DD} is increased in CMOS circuits.
(x) What is the advantage of the R-2R ladder DAC over the weighted-resistor type DAC? (10 × 2)

SECTION – B

2 (i) Perform (– 48 – 23) using 2's complement Method. Use 8-bit representation. 4
(ii) What is Gray code? How is it constructed? Where is it used? Represent the decimal number 27 in Gray code. 4
(iii) The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word. 4

1001001011100111101100011011

(iv) Show that $A.B+\overline{(\overline{A+B})}=A\oplus B$. Implement the function using four NAND gates. 4

3 (i) Design a converter (gate level circuit) to convert BCD digit to its equivalent Gray code. 5
(ii) How is Priority Encoder different from simple encoder? What is the role of enable in decoders? 5

P.T.O.

(iii) Write the equations for 1-bit full adder. Realize a 1-bit full adder using (a) minimum-sized and minimum number of multiplexers (b) universal gates. 6

4 (i) Convert a D-flip-flop to RS flipflop. 5

(ii) What is a Universal shift Register? Draw the circuit and discuss its operation. 5

(iii) Design a mod-6 synchronous counter using JK flip-flops. What is the duty cycle for most significant stage? Is the counter self-starting? Illustrate with state diagram. 6

5 (i) A static RAM IC that has a circuitry of 1K × 1, one active-LOW chip select and separate data input and output. Show how to combine several of such ICs to form a 1K × 8 module. 4

(ii) Implement the following multiple input and multiple output function using (a) ROM, (b) PLD, and (c) PLA. 12

6 (i) Name and discuss the three types of TTL gates. How are TTL ICs interfaced with CMOS ICs. 8

(ii) Discuss 3 types of Analog-to-Digital Converters. Mention at least one advantage of each. 8

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