Roll No.

## Paper ID [A0210]

(Please fill this Paper ID in OMR Sheet)

## BCA (205) (S05) (O) (Sem. - $2^{\text {nd }}$ ) <br> DIGITAL CIRCUITS \& LOGIC DESIGN

## Time : 03 Hours

Maximum Marks : 75

## Instruction to Candidates:

1) Section - A is Compulsory.
2) Attempt any Nine questions from Section - B.

## Section - A

Q1)
$(15 \times 2=30)$
a) Convert the following hexadecimal numbers into decimal
(i) 3 FFE
(ii) 2180
b) (10101) convert to Decimal Number system.
c) What do you understand from propagation delay time?
d) What is the use of karnaugh maps?
e) What is the use of gray codes for number representation?
f) Differentiate between combinational and sequential circuits.
g) Give the advantages of edge triggered flip-flops.
h) What is a race around condition?
i) Explain NOR gate with truth table.
j) Write the working of 4: 1 multiplexer.
k) What is Encoder?

1) Give advantages and disadvantages of synchronous over asynchronous counters.
m) Give applications of shift registers.
n) Give four possible modes of operation for registers.
o) What is a ring counter?

## Section - B

$$
(9 \times 5=45)
$$

Q2) Draw the minimized logic circuit for the Boolean equation
$\mathrm{Y}=\mathrm{A}^{\prime} \mathrm{B}^{\prime} \mathrm{C}^{\prime} \mathrm{D}+\mathrm{AB} \mathrm{C}^{\prime} \mathrm{D}+\mathrm{ABC} \mathrm{C}^{\prime} \mathrm{D}+\mathrm{ABCD} \mathrm{A}^{\prime}$.

Q3) How are AND, OR and NOT operations realized with NAND gates?

Q4) Convert decimal no. 100.55 into binary, octal codes.

Q5) State and discuss the De-Morgan's Theorem's.

Q6) Draw the circuit of a 3 to 8 decoder and explain its operation.
Q7) Explain code converters with example.
Q8) Draw and explain full adder using two multiplexers.
Q9) Discuss the working of JK master slave flip-flop.

Q10) Write short note on error detecting and correcting codes.

Q11) Discuss the working of synchronous counter.

Q12) Explain working of asynchronous counter.

Q13) Draw and explain 4 bit bi-directional shift registers.

