Roll No. .....

Total No. of Questions : 13] **[Total No. of Pages : 02**

Paper ID [A0218]

(Please fill this Paper ID in OMR Sheet)

BCA (403) (S05) (O) (LE) (Sem. - 4th)

COMPUTER SYSTEM ARCHITECTURE

Time : 03 Hours **Maximum Marks : 75**

Instruction to Candidates:

1) Section - A is **Compulsory**.

2) Attempt any **Nine** questions from Section - B.

Section - A

Q1) ***(15 × 2 = 30)***

a) Draw the diagram of stored program organization.

b) Define effective address.

c) What are clock pulses?

d) What are the four phases of instruction cycle?

e) What is interrupt cycle?

f) What is stack pointer?

g) What do you mean by multiprogramming?

h) What is bootstrap loader?

i) What is memory address map?

j) Define hit ratio.

k) How can you write into cache?

l) What is the relation between address space and memory space in virtual memory system?

m) Define logical address.

n) Define I/O port.

o) What is DMA?

Section - B

(9 × 5 = 45)

Q2) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

Q3) Discuss the concept of common bus system.

Q4) Explain the block diagram of control unit.

Q5) Convert the following arithmetic expressions from reverse Polish notation to infix notation:

(a) A B C D E + * - /

(b) A B C D E * / - +

(c) A B C * / D – E F / +

(d) A B C D E F G + * + * + *

Q6) Explain different instruction formats.

Q7) Explain the architecture of the control unit.

Q8) Describe the memory hierarchy.

Q9) Describe the memory address map.

Q10) Discuss in detail the hardware organization of Associative memory.

Q11) Explain the associative mapping and the direct mapping of Cache memory.

Q12) Write a note on Segmented Page mapping.

Q13) Explain the I/O interface for transferring information between internal storage and external I/O devices.