Subject Code—4376-X

P.G.D.C.A. EXAMINATION

June, 2006

(First Semester)

(Re-appear)

MS-03

DIGITAL ELECTRONICS

Time : 3 *Hours* *Maximum Marks* : 100

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Why NAND and NOR gates are known as universal gates ? How can we implement AND, OR, NOT gate using NAND and NOR gate ? 10

   (b) State and prove De'Morgan's theorem. 5

   (c) Draw the truth table and logic diagram of EX-OR gate. 5

P.T.O.

2. (a) Minimize the following expression using K-map and realize with NAND gates.

$f(A, B, C, D) = \Sigma m\ (1, 3, 7, 11, 15) + d\ (0, 2, 5)$ 10

(b) What is Multiplexer ? Draw the logic diagram of 4 : 1 multiplexer with stroke input using NAND gates. 10

3. (a) What is Full Adder ? Draw the truth table and logic diagram of full adder using NAND gates. 10

(b) Perform the following subtraction using 2's complement method : 10

(i) $(110101)_2 - (10010)_2$

(ii) $(101101 \cdot 101)_2 - (10110 \cdot 01)_2$

(iii) $(1001 \cdot 01)_2 - (101101 \cdot 10)_2$

(iv) $(1 \cdot 001)_2 - (1011)_2$

4. (a) Define IC. Discuss the characteristics of digital IC's. 10

(b) Explain TTL logic family in detail. 10

5. (a) Discuss briefly the role of CMOS inverter and tristate buffer in digital system. 10

   (b) Draw the truth table and logic diagram of BCD to 7-segment decoder. 10

6. (a) Explain the race round problem in J-K flip-flop. How can it be solved ? 10

   (b) What is Shift Register ? Explain any *one* in detail. 10

7. Design a 3 bit synchronous binary UP/DOWN counter with a direction control M. Use J-K flip-flops. 20

8. (a) Explain the function of ROM chip in digital computers. 8

   (b) Draw the circuit of R-2R ladder type D/A converter and explain its operation. 12