E- JUN 2006

Subject Code—4273

M.C.A. (Second Year) EXAMINATION

June 2006

(5 Years Integrated Course)

(Re-appear)

MCA-204

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 *Hours* *Maximum Marks :* 100

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Design a 4-bit combinational circuit decrementor using four full adder circuit.

   (b) Draw the flow chart for instruction cycle.

P.T.O.

2. (a) Explain the function of the following memory reference instructions :
   (i) STA
   (ii) BUN
   (iii) BSA
   (iv) LDA

   (b) Draw and explain the process of address selection for control memory in microprogrammed control unit.

3. Design a microprogrammed control unit along with microprogrammed sequencer.

4. (a) List out the instructions of each type of addressing modes available.

   (b) Differentiate between different types of interrupts available in CPU.

5. Differentiate between the following :
   (a) RISC and CISC
   (b) Hardwired and Microprogrammed Control Unit.

6. Explain the following modes of data transfer techniques in CPU :
   (a) Progammed I/O
   (b) Interrupt Driven I/O
   (c) DMA.

7. (a) Discuss different mapping techniques in cache memory system.

   (b) Explain the concept of virtual memory system for execution of program.

8. Write short notes on the following :

   (a) Stack Organization

   (b) Shift Microoperations

   (c) Auxiliary Memory.