E- JUN 2006

Subject Code—4272

M.C.A. (Second Year) EXAMINATION

June 2006

(5 Years Integrated Course)

(Re-appear)

MCA-203

DIGITAL ELECTRONICS

Time : 3 *Hours* *Maximum Marks* : 100

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) State and prove De-Morgan's Theorems. 6

   (b) Explain NAND and NOR logic operations. 5

   (c) Obtain AND, OR and NOT operations using NOR operations. 9

P.T.O.

2. Do as directed : 20

(i) $(1001 \cdot 0101)_2 = (?)_{10}$

(ii) $(10 \cdot 625)_{10} = (?)_2$

(iii) $(6A28)_{16} = (?)_8$

(iv) $(327 \cdot 89)_{10} = (?)_{BCD\ CODE}$

(v) $(1101 \cdot 0110111)_2 = (?)_8$

(vi) $(15)_{10} - (8)_{10} = (?)$

(Using one's complement)

(vii) Find 2's complement of 01101

(viii) $(1100010)_2 \div (111)_2 = (?)_2$

(ix) $(1101101)_2 \times (101)_2 = (?)_2$

(x) $(-48)_{10} - (23)_{10}$ using 2's complement.

3. Simplify the following using K-maps : 20

(a) f (A, B, C, D) = πM (4, 5, 6, 7, 8, 12)

d (1, 2, 3, 9, 11, 14)

(b) f (A, B, C, D) = Σm (0, 3, 5, 6, 9, 10, 12, 15)

Also realize them using minimum number of gates.

4. (a) A BCD message appears in four input lines of a switching circuit. Design an AND, OR, NOT gate network which produces an output '1' whenever input combination is 0, 2, 3, 5 or 8.

(b) Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and one 2 to 4 line decoder. 10

5. (a) Explain the operation of master-slave J-K flip-flop with complete circuit arrangement and truth table. How the race around condition of J-K flip-flop is removed ? 15

(b) Show that J-K flip-flop can also be used as T and D flip-flops. 5

6. (a) Draw the diagram for universal shift register and explain its operation. 15

(b) Write a short note on Parity Generator/ Checker. 5

7. (a) Draw the diagram for 3 bit ripple counter and explain its operation with the help of waveforms. Use T flip-flop. 10

(b) Design a four bit decade counter (synchronous). Use J-K flip-flops. 10

8. (a) Explain various characteristics of digital IC's. 10

(b) Draw the circuit diagram for TTL Totem Pole NAND gate and explain its working. 10