M.C.A. COMPUTER SCIENCE - I

1.	The development of computers can be	divided into generations						
	(a) 3	(b) 4						
	(c) 5	(d) 6						
	× /							
2.	Choose the odd one out							
	(a) Micro computer	(b) Mini computer						
	(c) Super computer	(d) Digital computer						
3.	The electronic computer was the first computer that had used the stored program concept							
	introduced by John Von Neumann.							
	(a) UNIVAC	(b) EDSAC						
	(c) ENIAC	(d) EDVAC						
4.	In the development of logarithms,	had also played a key role.						
	(a) Napier	(b) Blaise Pascal						
	(c) J.M.Jacquard	(d) Charles Babbage						
5.	5. The main distinguishing feature of fifth generation computers will be							
	(a) Liberal use of microprocessors							
	(c) Extremely low cost	(d) Versatility						
	•							
6.	The computer that is not considered as							
	(a) Laptop computer	(b) Notebook computer						
	(c) Mini computer	(d) None of these						
7								
7.	The unit of speed used for super comp (a) KELOPS	(b) MELOPS						
	(a) KELOPS (c) GELOPS	(d) None of these						
	(c) GELOFS	(d) None of these						
8.	UNIVAC is an example of							
	(a) First generation computer	(b) Second generation computer						
	(c) Third generation computer	(d) Fourth generation computer						
9.	The unit that performs the arithmetic	cal and logical operations on the stored numbers is known as						
	(a) Arithmetic Logic Unit	(b) Control Unit						
	(c) Memory Unit	(d) Both (a) and (b)						
10.	The is the 'administrative' se							
	(a) Input Unit	(b) Output Unit						
	(c) Memory Unit	(d) Central Processing Unit						
11								
11.	Roman number system is a	(h) Non modifiered much on motors						
	(a) Positional number system	(b) Non-positional number system(d) None of these						
	(c) Both (a) and (b)	(d) None of these						
12.	The number system on which the modern computers operate							
1	(a) Decimal number system	(b) Octal number system						
	(c) Binary number system	(d) Hexadecimal number system						
13.	The binary equivalent of $(231)_{10}$ is							
	(a) 11100111	(b) 10111001						

14. The binary coding system that represents 246 different characters or bit combination is (a) BCD (b) ASCII (c) EBCDIC (d) Both (b) and (c) 15. The complement of the binary number 11001011 is (a) 1010100 (b) 00110100 (c) 00110101 (d) 00101100 16. The octal addition of (25) ₈ and (15) ₈ is: (a) (42)₈ (b) (40)₈ (c) (41)₈ (d) None of these 17. The hexadecimal subtraction of (56) ₁₆ from (427) ₁₆ results in (a) (3B1)₁₆ (b) (331)₁₆ (c) (371)₁₆ (d) (3D1)₁₆ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 		(c) 01110011	(d) None of these					
(a) 1010101 (b) 00110100 (c) 00110101 (d) 00101100 16. The octal addition of $(25)_8$ and $(15)_8$ is: (a) $(42)_8$ (b) $(40)_8$ (c) $(41)_8$ (d) None of these 17. The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in (a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND	14.	(a) BCD	(b) ASCII					
(c) 00110101 (d) 00101100 16. The octal addition of $(25)_8$ and $(15)_8$ is: (a) $(42)_8$ (b) $(40)_8$ (c) $(41)_8$ (d) None of these 17. The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in (a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND	15.	1						
16. The octal addition of $(25)_8$ and $(15)_8$ is: (a) $(42)_8$ (b) $(40)_8$ (c) $(41)_8$ (d) None of these 17. The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in (a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND								
(a) $(42)_8$ (b) $(40)_8$ (c) $(41)_8$ (d) None of these 17. The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in (a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND		(c) 00110101	(d) 00101100					
(a) $(42)_8$ (b) $(40)_8$ (c) $(41)_8$ (d) None of these17. The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in(a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18. A gate, which is also known as <i>inverter</i> is(a) AND(b) OR(c) NOT(d) NAND19. The output of a NAND Gate is 1, when(a) All inputs are 1(b) Any one input is 0(c) All inputs are 0(d) None of these20. The gates that are considered as universal gates are(a) OR and NOT(b) Only NOR(c) NAND and NOR(d) Only NAND	16.	The octal addition of $(25)_8$ and $(15)_8$ is:						
(c) $(41)_8$ (d) None of these17.The hexadecimal subtraction of $(56)_{16}$ from $(427)_{16}$ results in (a) $(3B1)_{16}$ (b) $(331)_{16}$ (c) $(371)_{16}$ (d) $(3D1)_{16}$ 18.A gate, which is also known as <i>inverter</i> is (a) AND(b) OR (c) NOT(d) NAND19.The output of a NAND Gate is 1, when (a) All inputs are 1 (c) All inputs are 0(b) Any one input is 0 (c) All inputs are 020.The gates that are considered as universal gates are (a) OR and NOT (c) NAND and NOR(d) Only NOR (d) Only NAND								
 (a) (3B1)₁₆ (b) (331)₁₆ (c) (371)₁₆ (d) (3D1)₁₆ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 								
 (a) (3B1)₁₆ (b) (331)₁₆ (c) (371)₁₆ (d) (3D1)₁₆ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 	17	The hexadecimal subtraction of $(56)_{12}$	from $(427)_{12}$ results in					
 (c) (371)₁₆ (d) (3D1)₁₆ 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 	17.							
 18. A gate, which is also known as <i>inverter</i> is (a) AND (b) OR (c) NOT (d) NAND 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 			(d) (2D1)					
 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 								
 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 	18.	A gate, which is also known as <i>inverte</i>	ris					
 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 			(b) OR					
 19. The output of a NAND Gate is 1, when (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 		(c) NOT	(d) NAND					
 (a) All inputs are 1 (b) Any one input is 0 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 								
 (c) All inputs are 0 (d) None of these 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 	19.	1						
 20. The gates that are considered as universal gates are (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 								
 (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 		(c) All inputs are 0	(d) None of these					
 (a) OR and NOT (b) Only NOR (c) NAND and NOR (d) Only NAND 	20	The gates that are considered as universal gates are						
(c) NAND and NOR (d) Only NAND	20.							
ANSWEDS								
ANSWEDS								
			A NISW/EDS					

	ANJWERJ									
1.	(c)	5.	(b)	9.	(a)	13.	(a)	17.	(d)	
2.	(d)	6.	(c)	10.	(d)	14.	(c)	18.	(c)	
3.	(d)	7.	(c)	11.	(b)	15.	(b)	19.	(b)	
4.	(a)	8.	(a)	12.	(c)	16.	(a)	20.	(c)	