DHARMSINH DESAI UNIVERSITY, NADIAD Third Sessional Examination [Semister : I (MCA)] Subject: Logical Organization of Computers

Date: 11-12-2008 Time: 1 Hour Max Marks:36

Q.1		[Marks : 12]
1	What is called negative edge triggering?	
2	LSI Provides, MSI Provides and VLSI Prov	vides
	maximum integrated gates.	
3	A set of instructions is called	
4	There are different flags available in 8085 Microproc	essor.
5	Multiple choice :	
	1 Data bus is a	
	a) Unidirectional b) Bidirectional c) Both	
	2 Control Bus has how many lines?	1
	a) 8-bits b) 16-bits c) None of the	above
	3 Stack pointer consists total number of bits are	
6	a) 8-bits b) 16-bits c) 32-bits	
6	State True or False (Justify)	
	1) Program counter register store address of instructions	
	2) Two-Byte instructions stores opcode and operand in same memo	ry location
7	3) In ripple counter pass clock signals to each flip flop	
7	Match following table	
	Instructions Hex Code	
	ADD A 3EH MVI A 87H	
	MVI A 87H	
O2.	Answer the Following questions. [Any Three]	[Marks 12]
Q2. A	.	[Marks 12]
А	Discuss Master Slave Flip Flop with Diagram.	[Marks 12]
A B	Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates.	
А	Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples.	ample
A B C	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform response to the set of the set of	ample ead operation.
A B C D	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples a block diagram of RAM Memory unit and how to perform rewise What is meant by Microprocessor? Draw 8085 microprocessor Hard 	ample ead operation.
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A B C D E	Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate exa Draw a block diagram of RAM Memory unit and how to perform re What is meant by Microprocessor? Draw 8085 microprocessor Hard and explain functionality of each.	ample ead operation.
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A B C D E Q3.	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples a block diagram of RAM Memory unit and how to perform rewhat is meant by Microprocessor? Draw 8085 microprocessor Hard and explain functionality of each. Answer the Following questions. Draw block diagram of memory cell 	ample ead operation. dware model [Marks : 12] [02]
A B C D E Q3. A	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples a block diagram of RAM Memory unit and how to perform rewind the set of the set of	ample ead operation. dware model [Marks : 12] [02]
A B C D E Q3. A B	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform rewith the second s	ample ead operation. dware model [Marks : 12] [02] tes. [05]
A B C D E Q3. A B	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform rewind the set of the	ample ead operation. dware model [Marks : 12] [02] tes. [05]
A B C D E Q3. A B C	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform rewith the set of the	ample ead operation. dware model [Marks : 12] [02] tes. [05]
A B C D E Q3. A B C	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform rewith the set of the	ample ead operation. dware model [Marks : 12] [02] tes. [05] [05]
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A B C D E Q3. A B C A	 Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate examples of RAM Memory unit and how to perform rewith a block diagram of RAM Memory unit and how to perform rewith a block diagram of RAM Memory unit and how to perform rewith a propriate by Microprocessor? Draw 8085 microprocessor Hard and explain functionality of each. Answer the Following questions. Draw block diagram of memory cell Discuss 4-bit binary Synchronous counter with appropriate logic gate. Draw architecture of 8085 MPU and explain it. OR Check the addressing modes of the following instructions 1) LDAX B 2) LXI SP, 2000H 3) MOV A, B 4) LDA Write a program to add two 8-bit data from memory location 0030H 	ample ead operation. dware model [Marks : 12] [02] tes. [05] [05] A 2000H [02] H and 0031H.
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A B C D E Q3. A B C A B	Discuss Master Slave Flip Flop with Diagram. Discuss BCD Ripple counter with appropriate logic gates. Explain data transfer and branch instruction set with appropriate exact Draw a block diagram of RAM Memory unit and how to perform react What is meant by Microprocessor? Draw 8085 microprocessor Hard and explain functionality of each. Answer the Following questions. Draw block diagram of memory cell Discuss 4-bit binary Synchronous counter with appropriate logic gat Draw architecture of 8085 MPU and explain it. OR Check the addressing modes of the following instructions 1) LDAX B 2) LXI SP, 2000H 3) MOV A,B 4) LDA Write a program to add two 8-bit data from memory location 0030F Store result in accumulator register and Draw flowchart. What is meant by shift register?	ample ead operation. dware model [Marks : 12] [02] tes. [05] [05] A 2000H [02] H and 0031H. [05]