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B. E. (Fourth Semester) Examination,
April-May, 2008

(AEI, EE, EI, Et & T Engg. Branch)

DIGITAL ELECTRONIC CIRCUITS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Part (a) of every unit is compulsory. Attempt any two part of (b), (c) and (d) from every unit.

Unit-I

1. (a) Define weighted and non-weighted code with suitable example. 2

   (b) Describe De Morgan's theorem and explain describing their proof 7

(2)

4. (a) Explain Gray to Binary code conversion and convert the binary number (1356)$_{10}$ into Gray code. 7

(b) Simplify the Boolean expression and draw the logic diagram: 7

$$X'Y'Z + X'YZ + XY'Z + XYZ' + XYZ$$

$$X'YZ + XY'Z$$

Unit-II

2. (a) Simplify the expression in standard SOP form: 7

$$Y = A(B + \bar{C}) + (AC')(B + \bar{C}A)$$

(b) Reduce the following four variable function using K-Map and implement it by NAND gate: 7

$$F = \sum m(0, 4, 12, 8, 5, 9, 7, 15)$$

(c) Simplify the following boolean function by K-Map: 7

$$F = \sum m(0, 1, 2, 3, 6, 7, 12, 14) + d(8, 9, 10, 15)$$

(d) Reduce the following boolean function by using tabular or Quine-McCluskey method: 7

$$F = \sum m(0, 1, 4, 5, 6, 15, 19, 22, 28)$$

Unit-III

(3)

2. (a) Explain the term Multiplexer and Demultiplexer. 7

(b) Design a 4-bit (Digit) BCD adder circuit. 7

(c) Describe the operation of 16-gram array logic with suitable example. 7

(d) Design a 4-bit comparator circuit. 7

Unit-IV

6. (a) "Flip-flop is a sequential circuit" Explain. 2

(b) Design S-R Flip Flop using NAND gate and describe the working with truth table. 7

(c) Design a 4-bit Asynchronous counter with a provision for up/down counting. 7

(d) Draw and describe the working of a parallel in serial out (PISO) shift register. Explain how a number can be shifted in and out from such register. 7

Unit-V

5. (a) Define the term Fan out with suitable example. 2

(b) Discuss interfacing of CMOS to TTL logic family. 7

(c) Draw and describe the basic operation and fabrication of IIL logic family. 7

(d) Explain the logic circuit of TTL. What is Totem-pole output. 7